Not Recommended For New Designs

BURR - BROWN®



PCM1604
PCM1605

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SoundPLUS™ 24-Bit, 192kHz Sampling,6-Channel, Enhanced Multi-Level, Delta-Sigma DIGITAL-TO-ANALOG CONVERTER

FEATURES

- PIN COMPATIBLE WITH PCM1600, PCM1601
- 24-BIT RESOLUTION
- ANALOG PERFORMANCE:
  Dynamic Range: 105dB typ
  SNR: 104dB typ
  THD+N: 0.0018% typ
  Full-Scale Output: 3.1Vp-p typ
- 8x OVERSAMPLING INTERPOLATION FILTER:
  Stopband Attenuation: –82dB
  Passband Ripple: ±0.002dB
- SAMPLING FREQUENCY: 10kHz to 200kHz
- ACCEPTS 16-, 18-, 20-, AND 24-BIT AUDIO DATA
- DATA FORMATS: Standard, I^2S, and Left-Justified
- SYSTEM CLOCK: 128/192/256/384/512/768f_S
- USER-PROGRAMMABLE FUNCTIONS:
  Digital Attenuation: 0dB to –63dB, 0.5dB/Step
  Soft Mute
  Zero Detect Mute
  Zero Flags May Be Used As General Purpose Logic Outputs
  Digital De-Emphasis
  Digital Filter Roll-Off: Sharp or Slow
- DUAL SUPPLY OPERATION:
  +5V Analog, +3.3V Digital
- 5V TOLERANT DIGITAL LOGIC INPUTS
- PACKAGES(1): LQFP-48 (PCM1604) and MQFP-48 (PCM1605)

APPLICATIONS

- INTEGRATED A/V RECEIVERS
- DVD MOVIE AND AUDIO PLAYERS
- HDTV RECEIVERS
- CAR AUDIO SYSTEMS
- DVD ADD-ON CARDS FOR HIGH-END PCs
- DIGITAL AUDIO WORKSTATIONS
- OTHER MULTI-CHANNEL AUDIO SYSTEMS

DESCRIPTION

The PCM1604(1) and PCM1605(1) are CMOS monolithic integrated circuits which feature six 24-bit audio digital-to-analog converters, and support circuitry in a small QFP-48 package. The digital-to-analog converters utilize Burr-Brown's enhanced multi-level, delta-sigma architecture, which employs 4th-order noise shaping and 8-level amplitude quantization to achieve excellent signal-to-noise performance, and a high tolerance to clock jitter.

The PCM1604 and PCM1605 accept industry-standard audio data formats with 16- to 24-bit audio data. Sampling rates up to 200kHz are supported. A full set of user-programmable functions are accessible through a 4-wire serial control port which supports register write and readback functions.

NOTE: (1) The PCM1604 and PCM1605 utilize the same die and are electrically identical. All references to the PCM1604 apply equally to the PCM1605.

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Twx: 910-952-1111 • Internet: http://www.burr-brown.com/ • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

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SBAS135

SPECIFICATIONS

All specifications at +25°C, $+V_{CC}$ = +5V, $+V_{DD}$ = +3.3V, system clock = $384f_S$ (f_S = 44.1kHz) and 24-bit data, unless otherwise noted.

PARAMETER	CONDITIONS	PCM1604Y, PCM1605Y MIN	TYP	MAX	UNITS
RESOLUTION			24		Bits
DATA FORMAT					
Audio Data Interface Formats	User Selectable		Standard, I²S, Left-Justified		
Data Bit Length	User Selectable		16, 18, 20, 24-Bit		
Audio Data Format			MSB-First, Binary Two's Complement		
Sampling Frequency (f_S)		10		200	kHz
System Clock Frequency			128, 192, 256, 384, 512, 768f_S		
DIGITAL INPUT/OUTPUT					
Logic Family			TTL-Compatible		
Input Logic Level					
V_{IH}		2.0			V
V_{IL}				0.8	V
Input Logic Current					
I_{IH}(1)	$V_{IN} = V_{DD}$			10	µA
I_{IL}(1)	V_{IN} = 0V			–10	µA
I_{IH}(2)	$V_{IN} = V_{DD}$		65	100	µA
I_{IL}(2)	V_{IN} = 0V			–10	µA
Output Logic Level					
V_{OH}(3)	I_{OH} = –4mA	2.4			V
V_{OL}(3)	I_{OL} = +4mA			1.0	V
DYNAMIC PERFORMANCE(4)					
THD+N, V_{OUT} = 0dB	f_S = 44.1kHz		0.0018	0.0045	%
	f_S = 96kHz		0.0035		%
V_{OUT} = –60dB	f_S = 44.1kHz		0.65		%
	f_S = 96kHz		0.75		%
Dynamic Range	EIAJ, A-Weighted, f_S =44.1kHz	100	105		dB
	A-Weighted, f_S = 96kHz		104		dB
Signal-to-Noise Ratio(5)	EIAJ, A-Weighted, f_S =44.1kHz	98	104		dB
	A-Weighted, f_S = 96kHz		103		dB
Channel Separation	f_S = 44.1kHz	96	102		dB
	f_S = 96kHz		101		dB
Level Linearity Error	V_{OUT} = –90dB		±0.5		dB
DC ACCURACY					
Gain Error			±1.0		% of FSR
Gain Mismatch, Channel-to-Channel			±1.0		% of FSR
Bipolar Zero Error	$V_O = 0.5V_{CC}$ at Bipolar Zero		±30		mV
ANALOG OUTPUT					
Output Voltage	Full Scale (0dB)		62% of V_{CC}		Vp-p
Center Voltage			50% V_{CC}		V
Load Impedance	AC Load	5			kΩ
DIGITAL FILTER PERFORMANCE					
Filter Characteristics, Sharp Roll-Off					
Passband	±0.002dB			0.454f_S	Hz
	–3dB			0.490f_S	Hz
Stopband		0.546f_S			Hz
Passband Ripple				±0.002	dB
Stopband Attenuation	Stopband = 0.546f_S	–75			dB
	Stopband = 0.567f_S	–82			dB
Filter Characteristics, Slow Roll-Off					
Passband	±0.002dB			0.274f_S	Hz
	–3dB			0.454f_S	Hz
Stopband		0.732f_S			Hz
Passband Ripple				±0.002	dB
Stopband Attenuation	Stopband = 0.732f_S	–82			dB
Delay Time			34/f_S		sec
De-Emphasis Error			±0.1		dB
ANALOG FILTER PERFORMANCE					
Frequency Response	f = 20kHz		–0.03		dB
	f = 44kHz		–0.20		dB

SPECIFICATIONS (Cont.)

All specifications at +25°C, $+V_{CC}$ = +5V, $+V_{DD}$ = +3.3V, system clock = $384f_S$ (f_S = 44.1kHz) and 24-bit data, unless otherwise noted.

PARAMETER	CONDITIONS	PCM1604Y, PCM1605Y MIN	TYP	MAX	UNITS
POWER SUPPLY REQUIREMENTS					
Voltage Range, V_{DD}		+3.0	+3.3	+3.6	V
V_{CC}		+4.5	+5.0	+5.5	V
Supply Current, I_{DD}(6)	f_S = 44.1kHz		20	28	mA
	f_S = 96kHz		42		mA
I_{CC}	f_S = 44.1kHz		40	56	mA
	f_S = 96kHz		42		mA
Power Dissipation	f_S = 44.1kHz		266	409	mW
	f_S = 96kHz		349		mW
TEMPERATURE RANGE					
Operation		–25		+85	°C
Storage		–55		+125	°C
Thermal Resistance, θ_{JA}			100		°C/W

NOTES: (1) Pins 38, 40, 41, 45-47 (SCKI, BCK, LRCK, DATA1, DATA2, DATA3). (2) Pins 34-37 (MDI, MC, ML, $\overline{RST}$). (3) Pins 1-6, 48 (ZERO1-6, ZEROA), Pin 39 (SCKO). (4) Analog performance specifications are tested with Shibasoku #725 THD Meter 400Hz HPF, 30kHz LPF on, average mode with 20kHz bandwidth limiting. The load connected to the analog output is 5kΩ or larger, AC-coupled. (5) SNR is tested with Infinite Zero Detection off. (6) SCKO is disabled.

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage, V_{DD}	+4.0V
V_{CC}	+6.5V
Digital Input Voltage	–0.2V to +5.5V
Digital Output Voltage(1)	–0.2V to (V_{DD} + 0.2V)
Input Current (except power supply)	±10mA
Power Dissipation	650mW
Operating Temperature Range	–25°C to +85°C
Storage Temperature	–55°C to +125°C
Lead Temperature (soldering, 5s)	+260°C
Package Temperature (IR reflow, 10s)	+235°C

NOTE: (1) Pin 33 (MDO) when output is disabled.



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

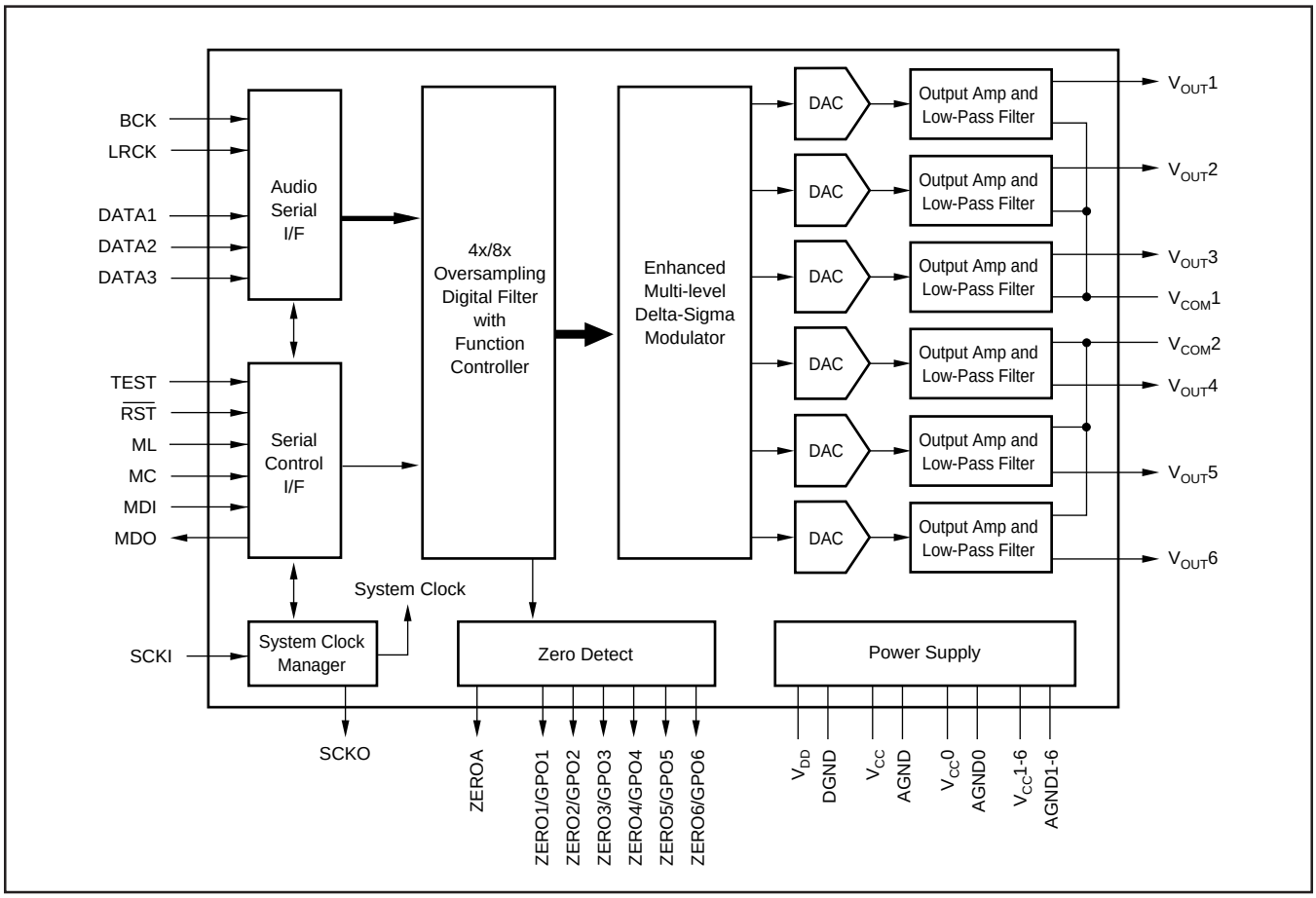
PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER(1)	TRANSPORT MEDIA
PCM1604Y	LQFP-48	340	–25°C to +85°C	PCM1604Y	PCM1604Y	250-Piece Tray
"	"	"	"	"	PCM1604Y/2K	Tape and Reel
PCM1605Y	MQFP-48	359	–25°C to +85°C	PCM1605Y	PCM1605Y	84-Piece Tray
"	"	"	"	"	PCM1605Y/1K	Tape and Reel

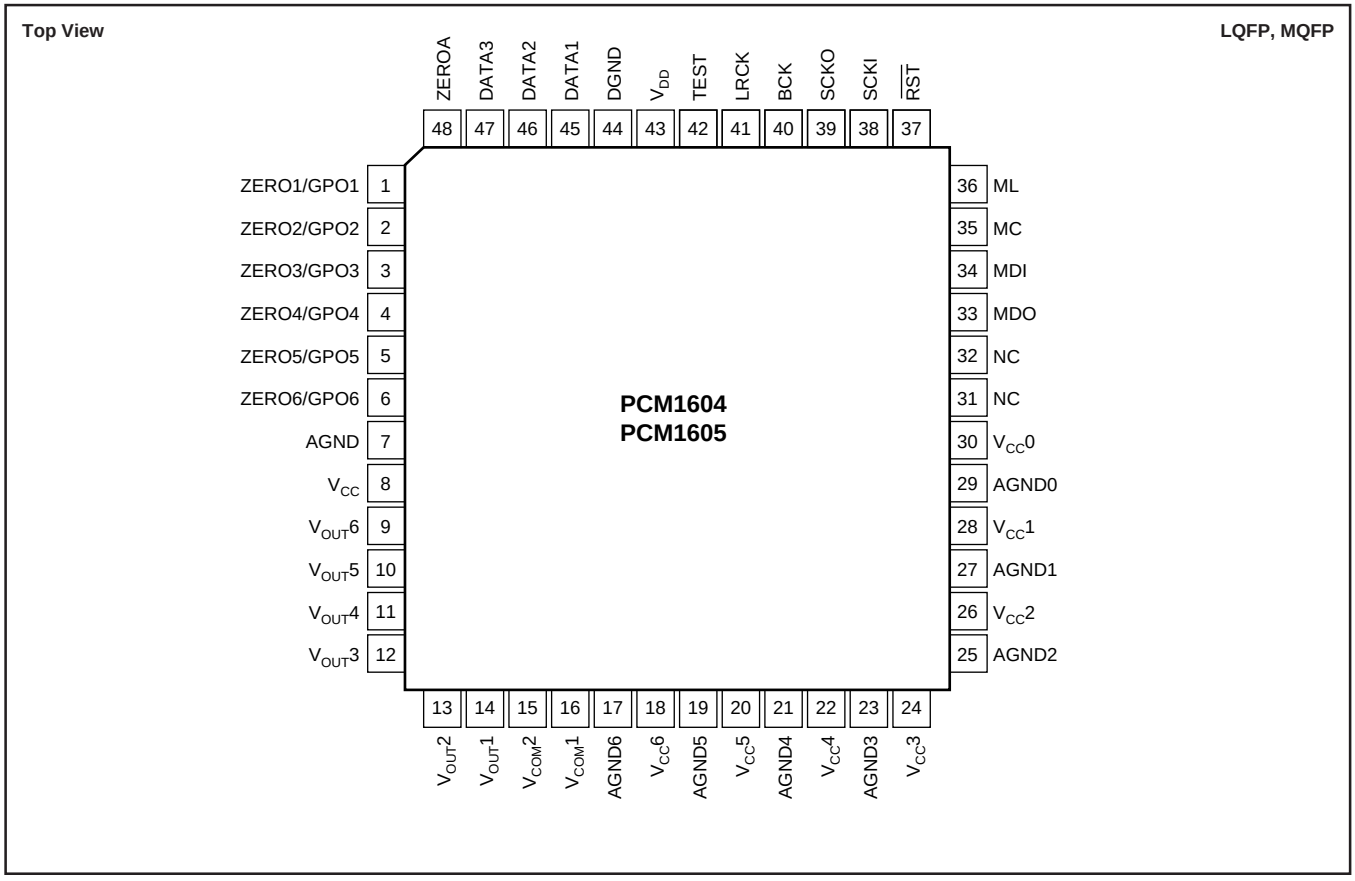
NOTE: (1) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /2K indicates 2000 devices per reel). Ordering 2000 pieces of "PCM1604Y/2K" will get a single 2000-piece Tape and Reel.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

BLOCK DIAGRAM



PIN CONFIGURATION



PIN ASSIGNMENTS

PIN	NAME	I/O	DESCRIPTION
1	ZERO1/GPO1	O	Zero Data Flag for $V_{OUT}1$. Can also be used as GPO pin.
2	ZERO2/GPO2	O	Zero Data Flag for $V_{OUT}2$. Can also be used as GPO pin.
3	ZERO3/GPO3	O	Zero Data Flag for $V_{OUT}3$. Can also be used as GPO pin.
4	ZERO4/GPO4	O	Zero Data Flag for $V_{OUT}4$. Can also be used as GPO pin.
5	ZERO5/GPO5	O	Zero Data Flag for $V_{OUT}5$. Can also be used as GPO pin.
6	ZERO6/GPO6	O	Zero Data Flag for $V_{OUT}6$. Can also be used as GPO pin.
7	AGND	—	Analog Ground
8	V_{CC}	—	Analog Power Supply, +5V
9	$V_{OUT}6$	O	Voltage Output for Audio Signal Corresponding to Rch on DATA3.
10	$V_{OUT}5$	O	Voltage Output for Audio Signal Corresponding to Lch on DATA3.
11	$V_{OUT}4$	O	Voltage Output for Audio Signal Corresponding to Rch on DATA2.
12	$V_{OUT}3$	O	Voltage Output for Audio Signal Corresponding to Lch on DATA2.
13	$V_{OUT}2$	O	Voltage Output for Audio Signal Corresponding to Rch on DATA1.
14	$V_{OUT}1$	O	Voltage Output for Audio Signal Corresponding to Lch on DATA1.
15	$V_{COM}2$	O	Common Voltage Output. This pin should be bypassed with a 10µF capacitor to AGND.
16	$V_{COM}1$	O	Common Voltage Output. This pin should be bypassed with a 10µF capacitor to AGND.
17	AGND6	—	Analog Ground
18	$V_{CC}6$	—	Analog Power Supply, +5V
19	AGND5	—	Analog Ground
20	$V_{CC}5$	—	Analog Power Supply, +5V
21	AGND4	—	Analog Ground
22	$V_{CC}4$	—	Analog Power Supply, +5V
23	AGND3	—	Analog Ground
24	$V_{CC}3$	—	Analog Power Supply, +5V
25	AGND2	—	Analog Ground
26	$V_{CC}2$	—	Analog Power Supply, +5V
27	AGND1	—	Analog Ground
28	$V_{CC}1$	—	Analog Power Supply, +5V
29	AGND0	—	Analog Ground
30	$V_{CC}0$	—	Analog Power Supply, +5V
31	NC	—	No Connection. Must be open.
32	NC	—	No Connection. Must be open.
33	MDO	O	Serial Data Output for Function Register Control Port[3]
34	MDI	I	Serial Data Input for Function Register Control Port[1]
35	MC	I	Shift Clock for Function Register Control Port[1]
36	ML	I	Latch Enable for Function Register Control Port[1]
37	$\overline{RST}$	I	System Reset, Active LOW[1]
38	SCKI	I	System Clock In. Input frequency is 128, 192, 256, 384, 512 or 768f_S.[2]
39	SCKO	O	Buffered Clock Output. Output frequency is 128, 192, 256, 384, 512, or 768f_S or one-half of 128, 192, 256, 384, 512, or 768f_S.
40	BCK	I	Shift Clock Input for Serial Audio Data[2]
41	LRCK	I	Left and Right Clock Input. This clock is equal to the sampling rate, f_S.[2]
42	TEST	—	Test Pin. This pin should be connected to DGND.[1]
43	V_{DD}	—	Digital Power Supply, +3.3V
44	DGND	—	Digital Ground for +3.3V
45	DATA1	I	Serial Audio Data Input for $V_{OUT}1$ and $V_{OUT}2$[2]
46	DATA2	I	Serial Audio Data Input for $V_{OUT}3$ and $V_{OUT}4$[2]
47	DATA3	I	Serial Audio Data Input for $V_{OUT}5$ and $V_{OUT}6$[2]
48	ZEROA	O	Zero Data Flag. Logical “AND” of ZERO1 through ZERO6.

NOTES: (1) Schmitt-Trigger input with internal pull-down, 5V tolerant. (2) Schmitt-Trigger input, 5V tolerant. (3) Tri-state output.

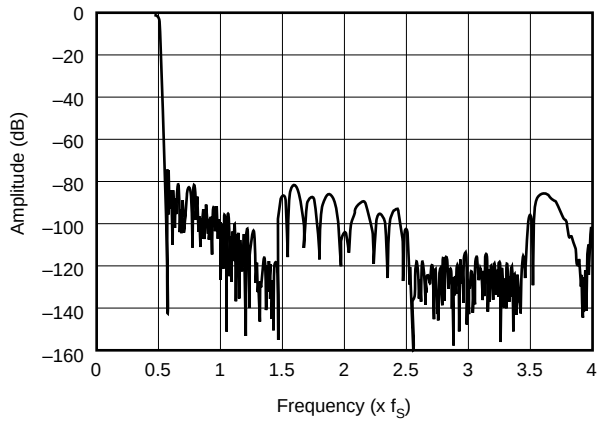
TYPICAL PERFORMANCE CURVES

All specifications at +25°C, V_{CC} = 5V, V_{DD} = 3.3V, SYSCLK = 384f_S (f_S = 44.1kHz), and 24-bit input data, unless otherwise noted.

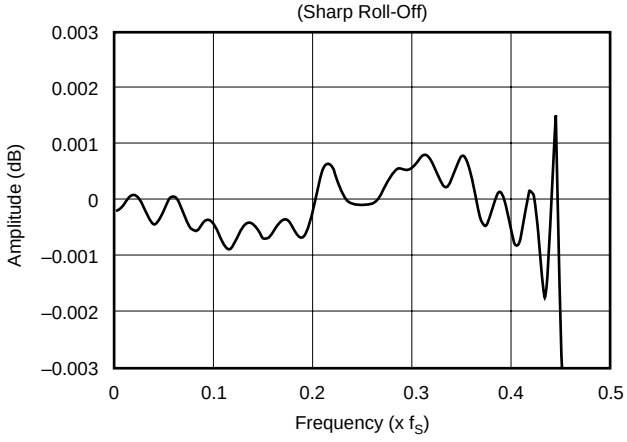
DIGITAL FILTER

Digital Filter (De-Emphasis Off, f_S = 44.1kHz)

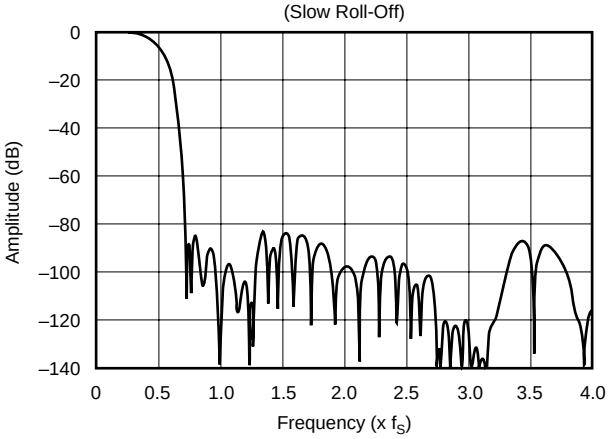
FREQUENCY RESPONSE
(Sharp Roll-Off)



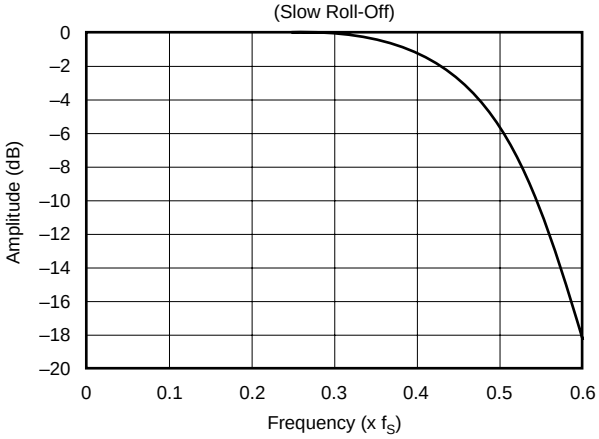
PASSBAND RIPPLE
(Sharp Roll-Off)



FREQUENCY RESPONSE
(Slow Roll-Off)

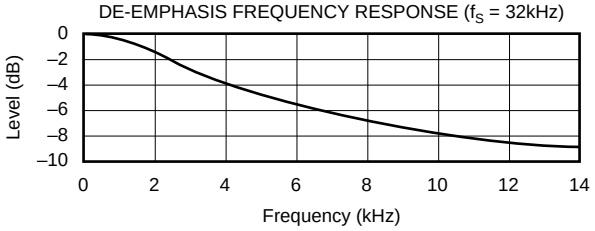


TRANSITION CHARACTERISTICS
(Slow Roll-Off)

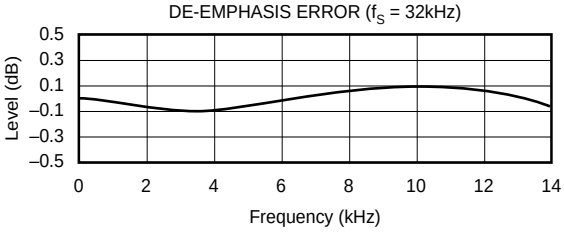


De-Emphasis Error

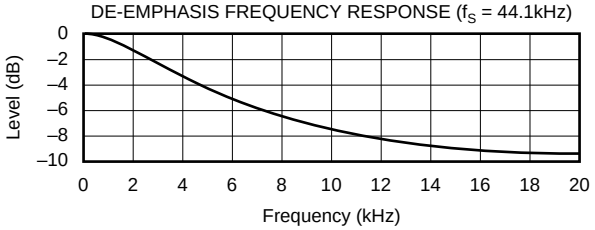
DE-EMPHASIS FREQUENCY RESPONSE (f_S = 32kHz)



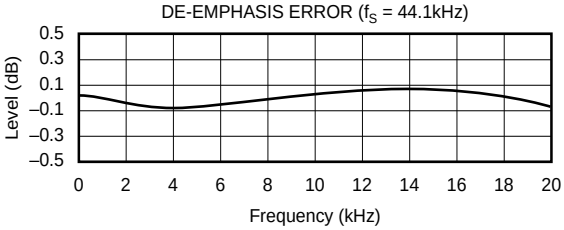
DE-EMPHASIS ERROR (f_S = 32kHz)



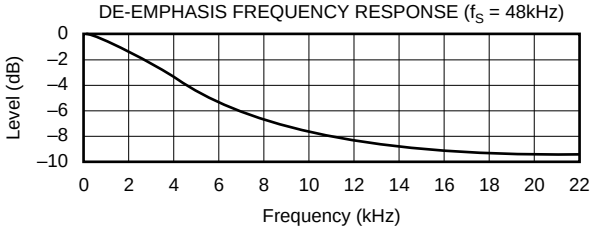
DE-EMPHASIS FREQUENCY RESPONSE (f_S = 44.1kHz)



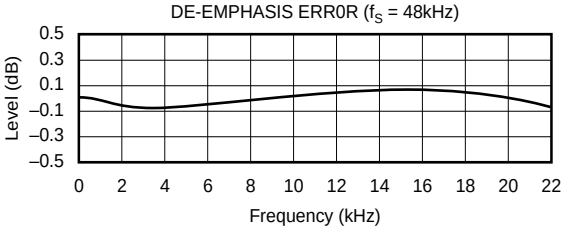
DE-EMPHASIS ERROR (f_S = 44.1kHz)



DE-EMPHASIS FREQUENCY RESPONSE (f_S = 48kHz)



DE-EMPHASIS ERR0R (f_S = 48kHz)



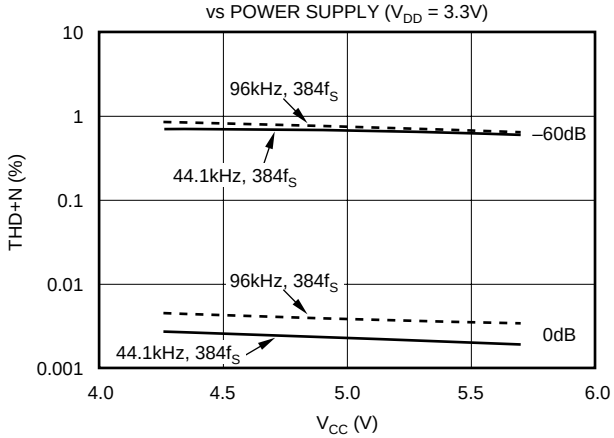
TYPICAL PERFORMANCE CURVES (Cont.)

All specifications at +25°C, V_{CC} = 5V, V_{DD} = 3.3V, SYSCLK = 384f_S (f_S = 44.1kHz), and 24-bit input data, unless otherwise noted.

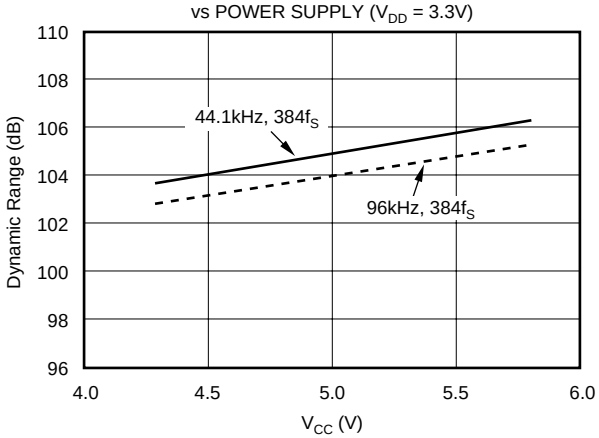
ANALOG DYNAMIC PERFORMANCE

Supply Voltage Characteristics

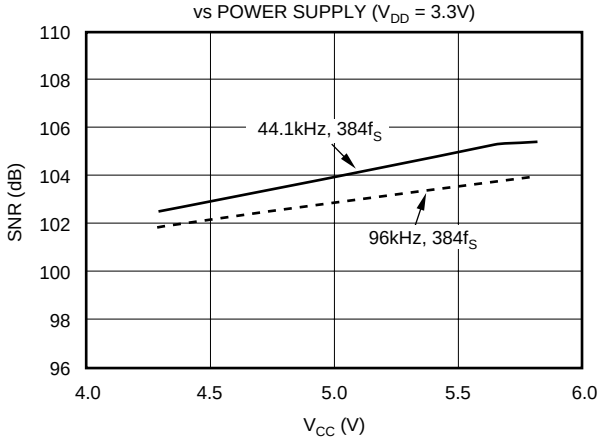
TOTAL HARMONIC DISTORTION + NOISE
vs POWER SUPPLY (V_{DD} = 3.3V)



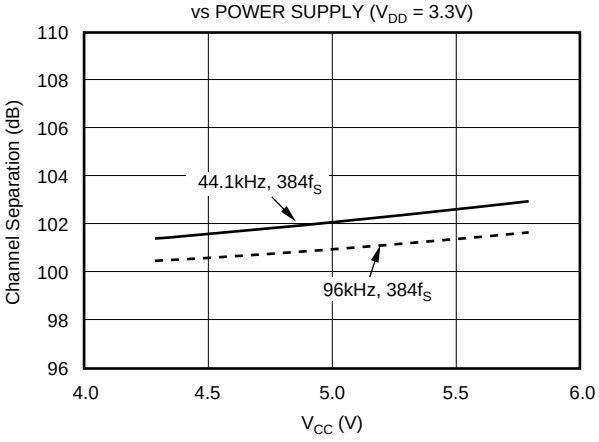
DYNAMIC RANGE
vs POWER SUPPLY (V_{DD} = 3.3V)



SIGNAL-TO-NOISE RATIO
vs POWER SUPPLY (V_{DD} = 3.3V)



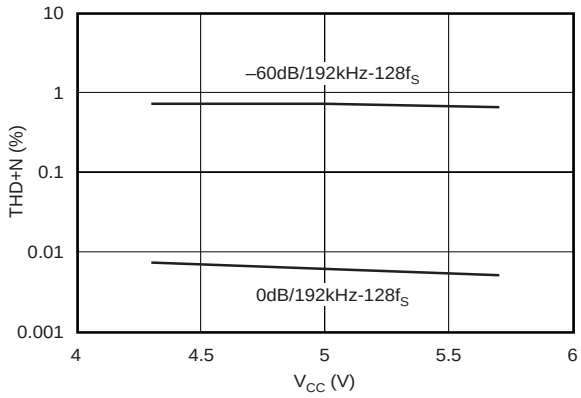
CHANNEL SEPARATION
vs POWER SUPPLY (V_{DD} = 3.3V)



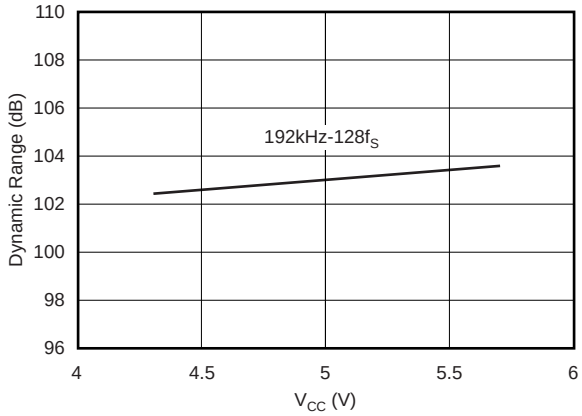
TYPICAL PERFORMANCE CURVES (Cont.)

All specifications at V_{DD} = +3.3V, 128f_S system clock, 64x oversampling, and 24-bit data. Only two channels (V_{OUT}1 and V_{OUT}2) are operated. All other channels are set to all zero input data and DAC operation is disabled (bits DAC3 through DAC6 of Register 8 are set to 1).

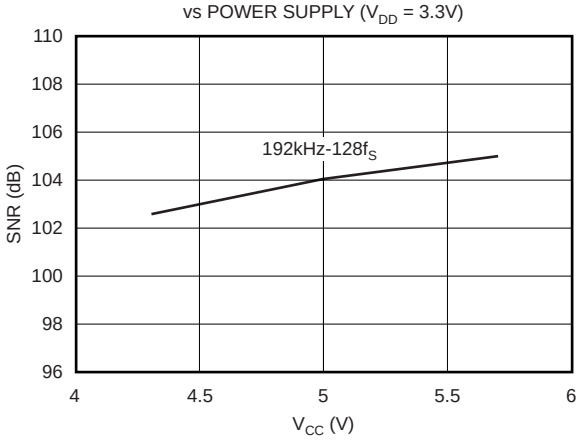
TOTAL HARMONIC DISTORTION + NOISE
vs POWER SUPPLY (V_{DD} = 3.3V)



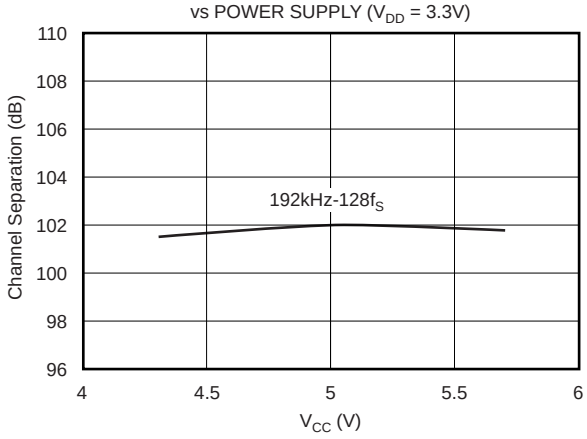
DYNAMIC RANGE
vs POWER SUPPLY (V_{DD} = 3.3V)



SIGNAL-TO-NOISE RATIO
vs POWER SUPPLY (V_{DD} = 3.3V)



CHANNEL SEPARATION
vs POWER SUPPLY (V_{DD} = 3.3V)



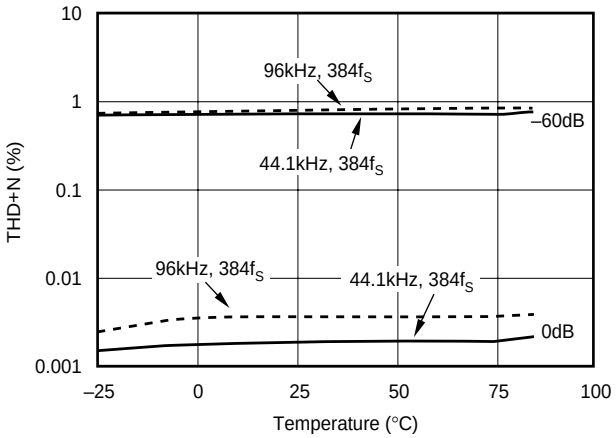
TYPICAL PERFORMANCE CURVES (Cont.)

All specifications at +25°C, V_{CC} = 5V, V_{DD} = 3.3V, SYSCLK = 384f_S (f_S = 44.1kHz), and 24-bit input data, unless otherwise noted.

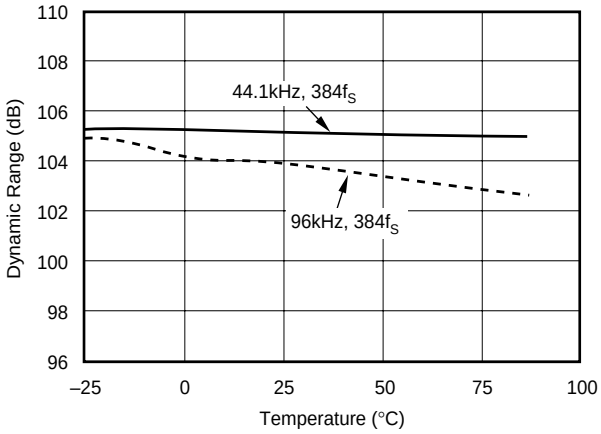
ANALOG DYNAMIC PERFORMANCE (Cont.)

Temperature Characteristics

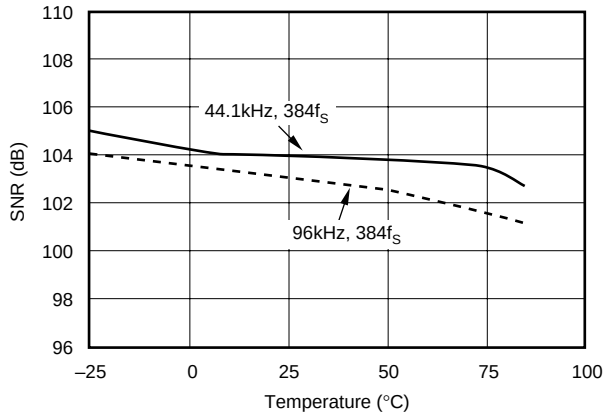
TOTAL HARMONIC DISTORTION + NOISE vs TEMPERATURE



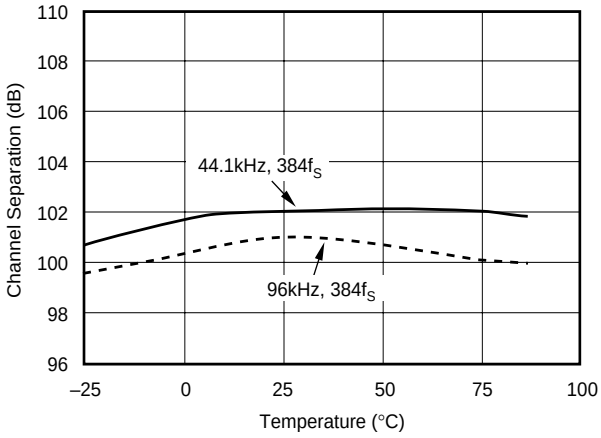
DYNAMIC RANGE vs TEMPERATURE



SIGNAL-TO-NOISE RATIO vs TEMPERATURE



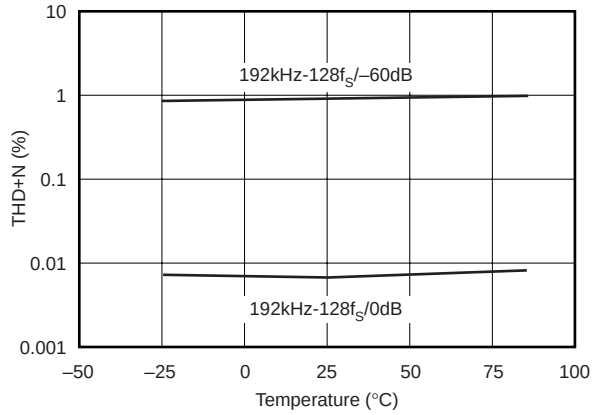
CHANNEL SEPARATION vs TEMPERATURE



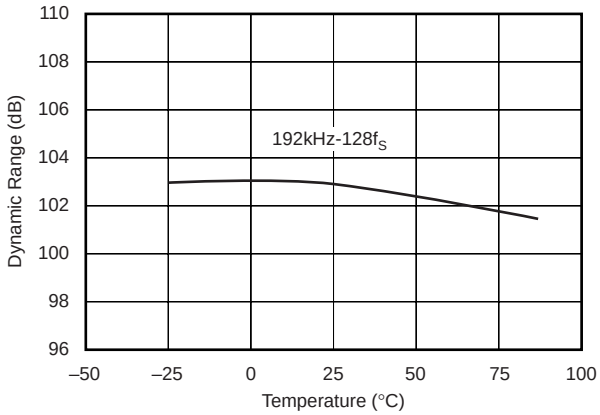
TYPICAL PERFORMANCE CURVES (Cont.)

All specifications at V_{CC} = +5V, V_{DD} = +3.3V, 128f_S system clock, 64x oversampling, and 24-bit data. Only two channels (V_{OUT}1 and V_{OUT}2) are operated. All other channels are set to all zero input data and DAC operation is disabled (bits DAC3 through DAC6 of Register 8 are set to 1).

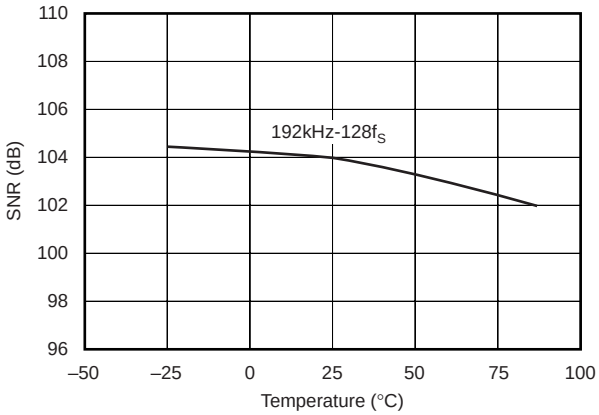
TOTAL HARMONIC DISTORTION + NOISE vs TEMPERATURE



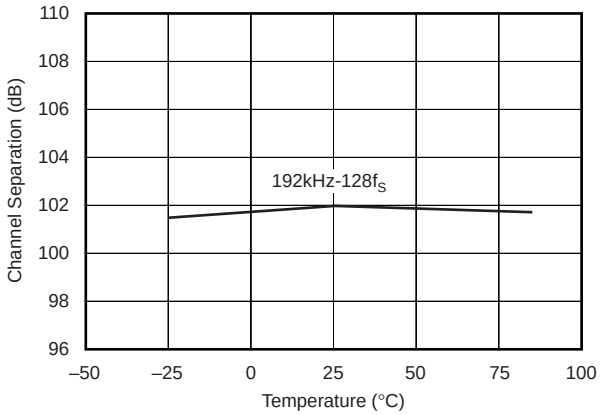
DYNAMIC RANGE vs TEMPERATURE



SIGNAL-TO-NOISE RATIO vs TEMPERATURE



CHANNEL SEPARATION vs TEMPERATURE



SYSTEM CLOCK AND RESET FUNCTIONS

SYSTEM CLOCK INPUT

The PCM1604 and PCM1605 require a system clock for operating the digital interpolation filters and multi-level delta-sigma modulators. The system clock is applied at the SCKI input (pin 38). Table I shows examples of system clock frequencies for common audio sampling rates.

Figure 1 shows the timing requirements for the system clock input. For optimal performance, it is important to use a clock source with low phase jitter and noise. Burr-Brown's PLL1700 multi-clock generator is an excellent choice for providing the PCM1604 system clock source.

To obtain optimal dynamic performance when operating with a 192kHz sampling frequency, it is recommended that only two channels be enabled for operation ($V_{OUT}1$ and $V_{OUT}2$). The remaining four channels should be disabled by setting bits DAC3 through DAC6 of control register 8 to logic 1 state.

SYSTEM CLOCK OUTPUT

A buffered version of the system clock input is available at the SCKO output (pin 39). SCKO can operate at either full (f_{SCKI}) or half ($f_{SCKI}/2$) rate. The SCKO output frequency may be programmed using the CLKD bit of Control Register 9. The SCKO output pin can also be enabled or disabled using the CLKE bit of Control Register 9. The default is SCKO enabled.

POWER-ON AND EXTERNAL RESET FUNCTIONS

The PCM1604 includes a power-on reset function. Figure 2 shows the operation of this function.

The system clock input at SCKI should be active for at least one clock period prior to $V_{DD} = 2.0V$. With the system clock active and $V_{DD} > 2.0V$, the power-on reset function will be enabled. The initialization sequence requires 1024 system clocks from the time $V_{DD} > 2.0V$. After the initialization period, the PCM1604 will be set to its reset default state, as described in the Mode Control Register section of this data sheet.

The PCM1604 also includes an external reset capability using the $\overline{RST}$ input (pin 37). This allows an external controller or master reset circuit to force the PCM1604 to initialize to its reset default state. For normal operation, $\overline{RST}$ should be set to a logic '1'.

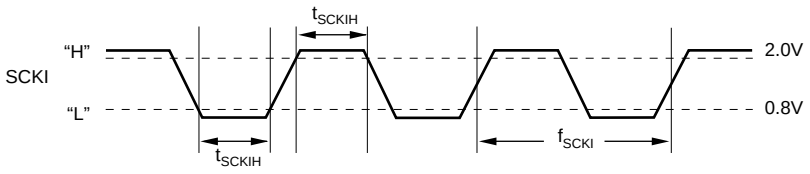
Figure 3 shows the external reset operation and timing. The $\overline{RST}$ pin is set to logic '0' for a minimum of 20ns. The $\overline{RST}$ pin is then set to a logic '1' state, which starts the initialization sequence, which lasts for 1024 system clock periods. After the initialization sequence is completed, the PCM1604 will be set to its reset default state, as described in the Mode Control Registers section of this data sheet.

The external reset is especially useful in applications where there is a delay between PCM1604 power up and system clock activation. In this case, the $\overline{RST}$ pin should be held at a logic '0' level until the system clock has been activated.

SAMPLING FREQUENCY (f_S)	SYSTEM CLOCK FREQUENCY (f_{SCKI}) (MHz)					
	$128f_S$	$192f_S$	$256f_S$	$384f_S$	$512f_S$	$768f_S$
16kHz	—	—	4.0960	6.1440	8.1920	12.2880
32kHz	—	—	8.1920	12.2880	16.3840	24.5760
44.1kHz	—	—	11.2896	16.9344	22.5792	33.8688
48kHz	—	—	12.2880	18.4320	24.5760	36.8640
88.2kHz	—	—	22.5792	33.8688	45.1584	See Note 1
96kHz	12.2880	18.4320	24.5760	36.8640	49.1520	See Note 1
176.4kHz	22.5792	33.8688	See Note 2	See Note 2	See Note 2	See Note 2
192	24.5760	36.8640	See Note 2	See Note 2	See Note 2	See Note 2

NOTE: (1) The $768f_S$ system clock rate is not supported for $f_S > 64kHz$. (2) This system clock rate is not supported for the given sampling frequency.

TABLE I. System Clock Rates for Common Audio Sampling Frequencies.



System Clock Pulse Width High t_{SCKIH} : 7ns min
System Clock Pulse Width Low t_{SCKIL} : 7ns min

FIGURE 1. System Clock Input Timing.

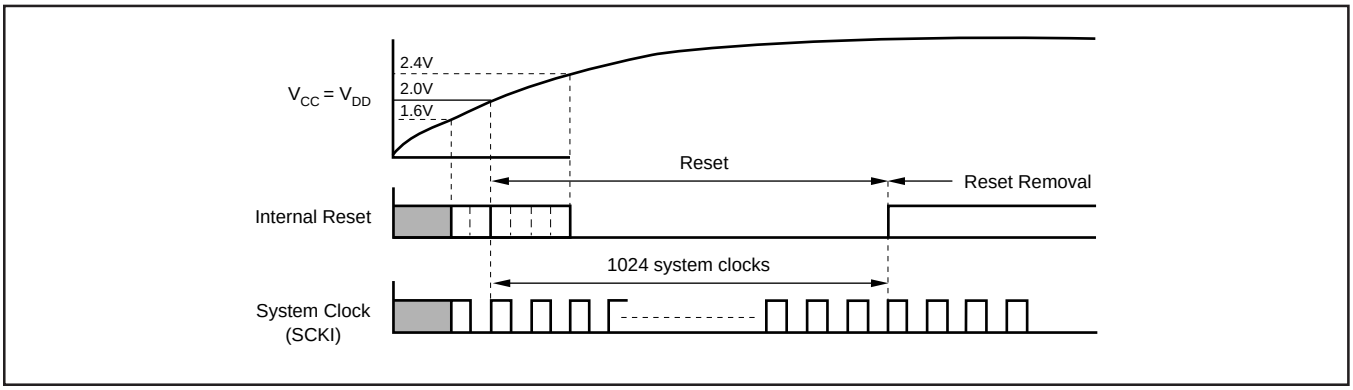


FIGURE 2. Power-On Reset Timing.

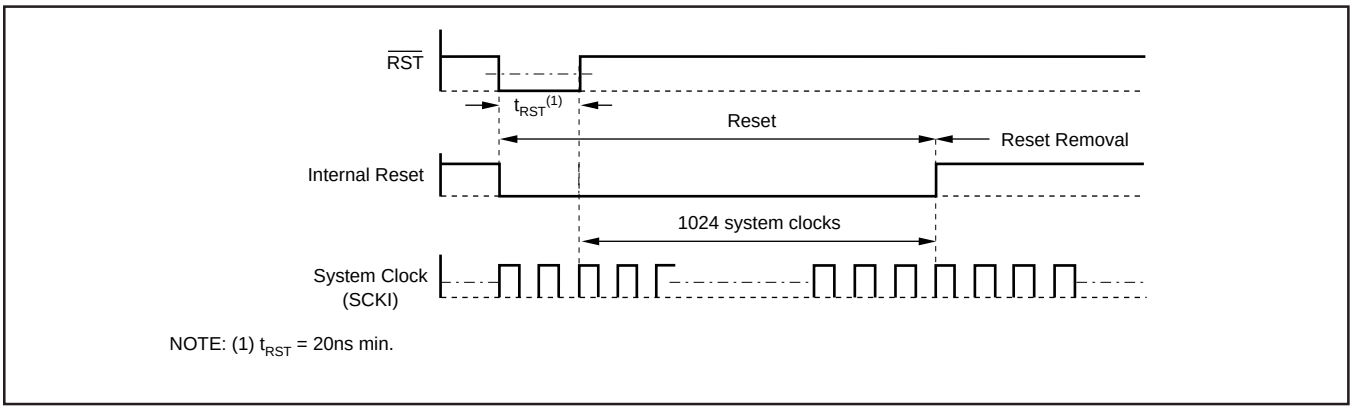


FIGURE 3. External Reset Timing.

AUDIO SERIAL INTERFACE

The audio serial interface for the PCM1604 is comprised of a 5-wire synchronous serial port. It includes LRCK (pin 41), BCK (pin 40), DATA1 (pin 45), DATA2 (pin 46) and DATA3 (pin 47). BCK is the serial audio bit clock, and is used to clock the serial data present on DATA1, DATA2 and DATA3 into the audio interface's serial shift registers. Serial data is clocked into the PCM1604 on the rising edge of BCK. LRCK is the serial audio left/right word clock. It is used to latch serial data into the serial audio interface's internal registers.

Both LRCK and BCK must be synchronous to the system clock. Ideally, it is recommended that LRCK and BCK be derived from the system clock input or output, SCKI or SCKO. The left/right clock, LRCK, is operated at the sampling frequency (f_S). The bit clock, BCK, may be operated at 48 or 64 times the sampling frequency.

AUDIO DATA FORMATS AND TIMING

The PCM1604 supports industry-standard audio data formats, including Standard, I^2S, and Left-Justified. The data formats are shown in Figure 4. Data formats are selected using the format bits, FMT[2:0], in Control Register 9. The default data format is 24-bit Standard. All formats require Binary Two's Complement, MSB-first audio data. Figure 5 shows a detailed timing diagram for the serial audio interface.

DATA1, DATA2 and DATA3 each carry two audio channels, designated as the Left and Right channels. The Left channel data always precedes the Right channel data in the serial data stream for all data formats. Table II shows the mapping of the digital input data to the analog output pins.

DATA INPUT	CHANNEL	ANALOG OUTPUT
DATA1	Left	$V_{OUT}1$
DATA1	Right	$V_{OUT}2$
DATA2	Left	$V_{OUT}3$
DATA2	Right	$V_{OUT}4$
DATA3	Left	$V_{OUT}5$
DATA3	Right	$V_{OUT}6$

TABLE II. Audio Input Data to Analog Output Mapping.

SERIAL CONTROL INTERFACE

The serial control interface is a 4-wire synchronous serial port which operates asynchronously to the serial audio interface. The serial control interface is utilized to program and read the on-chip mode registers. The control interface includes MDO (pin 33), MDI (pin 34), MC (pin 35), and ML (pin 36). MDO is the serial data output, used to read back the values of the mode registers; MDI is the serial data input, used to program the mode registers; MC is the serial bit clock, used to shift data in and out of the control port and ML is the control port latch clock.

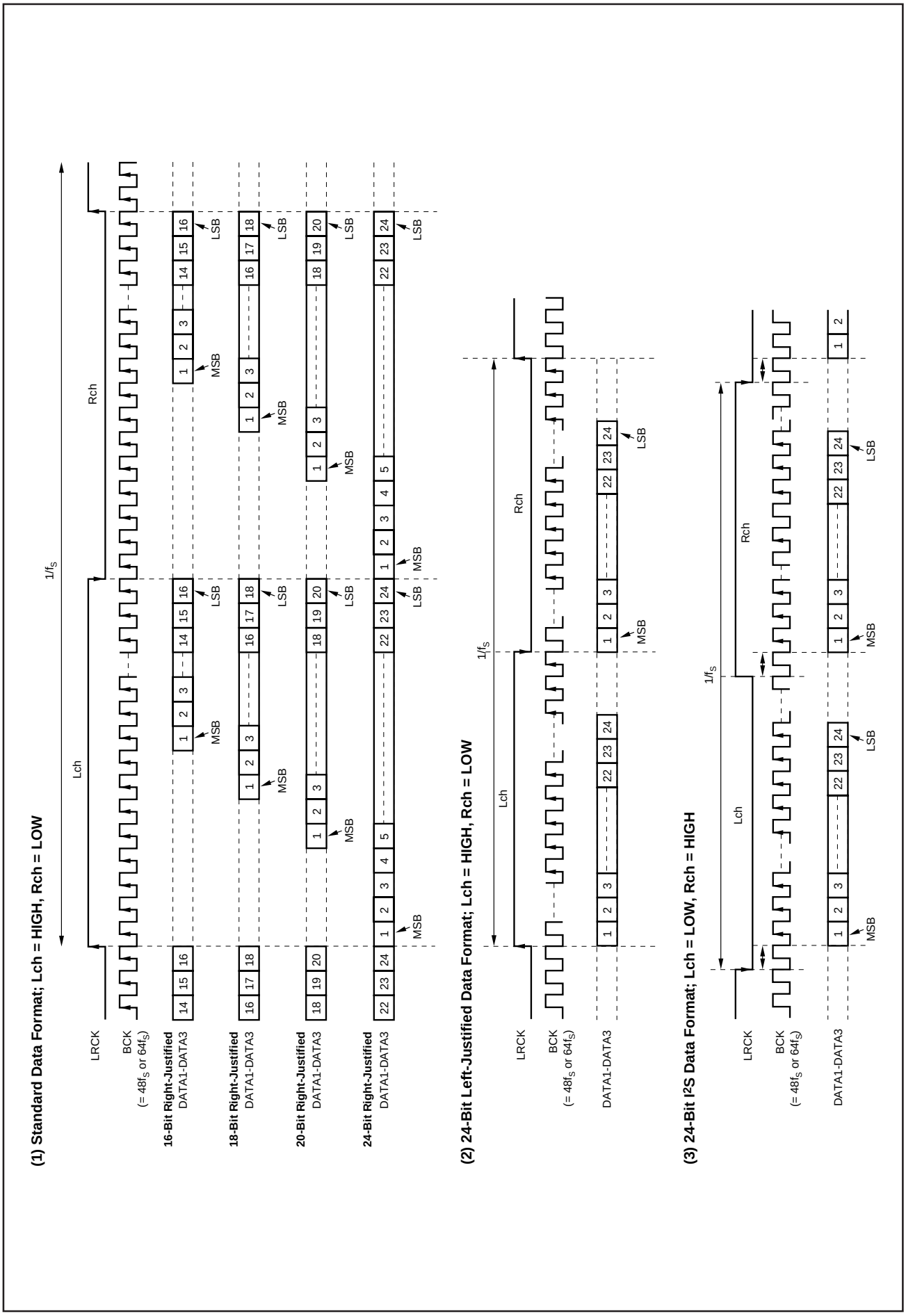
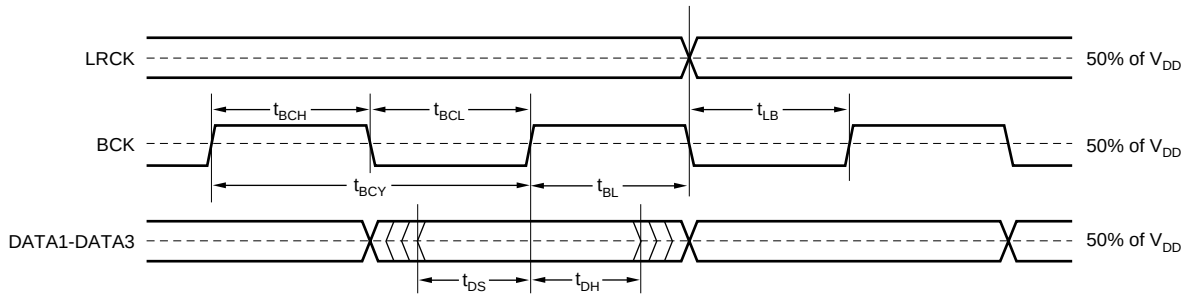


FIGURE 4. Audio Data Input Formats.



SYMBOL	PARAMETER	MIN	MAX	UNITS
t_{BCY}	BCK Pulse Cycle Time		48 or 64f_S(1)	
t_{BCH}	BCK High Level Time	35		ns
t_{BCL}	BCK Low Level Time	35		ns
t_{BL}	BCK Rising Edge to LRCK Edge	10		ns
t_{LB}	LRCK Falling Edge to BCK Rising Edge	10		ns
t_{DS}	DIN Set Up Time	10		ns
t_{DH}	DIN Hold Time	10		ns

NOTE: (1) f_S is the sampling frequency (e.g., 44.1kHz, 48kHz, 96kHz, etc.)

FIGURE 5. Audio Interface Timing.

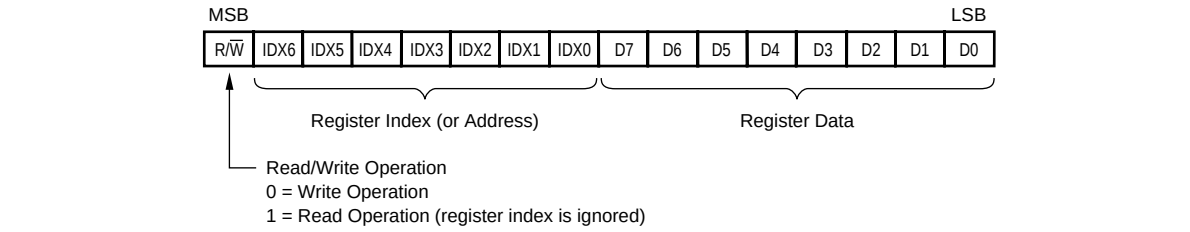


FIGURE 6. Control Data Word Format for MDI.

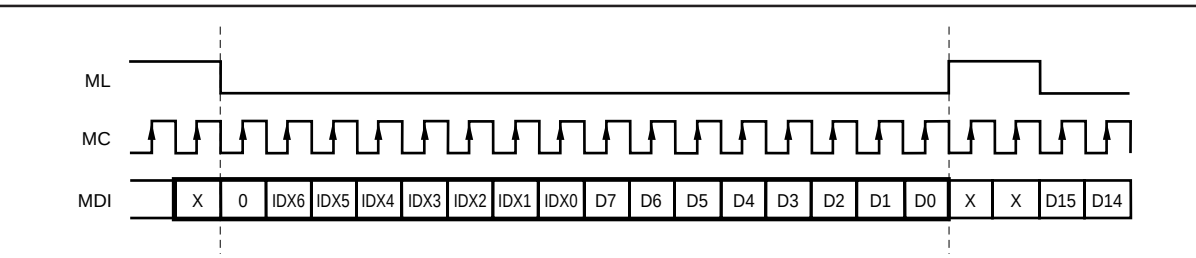


FIGURE 7. Write Operation Timing.

REGISTER WRITE OPERATION

All Write operations for the serial control port use 16-bit data words. Figure 6 shows the control data word format. The most significant bit is the Read/Write (R/W) bit. When set to '0', this bit indicates a Write operation. There are seven bits, labeled IDX[6:0], that set the register index (or address) for the Write operation. The least significant eight bits, D[7:0], contain the data to be written to the register specified by IDX[6:0].

Figure 7 shows the functional timing diagram for writing the serial control port. ML is held at a logic '1' state until a register needs to be written. To start the register write cycle, ML is set to logic '0'. Sixteen clocks are then provided on MC, corresponding to the 16-bits of the control data word on MDI. After the sixteenth clock cycle has completed, ML is set to logic '1' to latch the data into the indexed mode control register.

SINGLE REGISTER READ OPERATION

Read operations utilize the 16-bit control word format shown in Figure 6. For Read operations, the Read/Write (R/W) bit is set to '1'. Read operations ignore the index bits, IDX[6:0], of the control data word. Instead, the REG[6:0] bits in Control Register 11 are used to set the index of the register that is to be read during the Read operation. Bits IDX[6:0] should be set to 00_H for Read operations.

Figure 8 details the Read operation. First, Control Register 11 must be written with the index of the register to be read back. Additionally, the INC bit must be set to logic '0' in order to disable the Auto-Increment Read function. The Read cycle is then initiated by setting ML to logic '0' and setting the R/W bit of the control data word to logic '1', indicating a Read operation. MDO remains at a high-impedance state until the

Not Recommended For New Designs

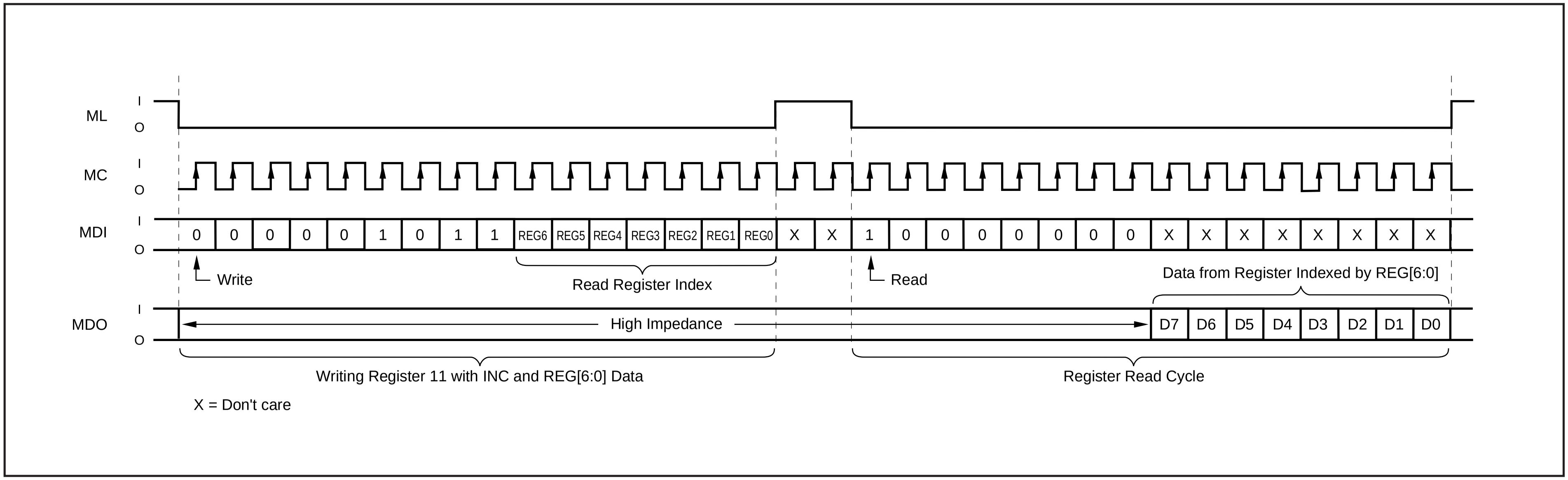


FIGURE 8. Read Operation Timing with INC = 0 (Single Register Read).

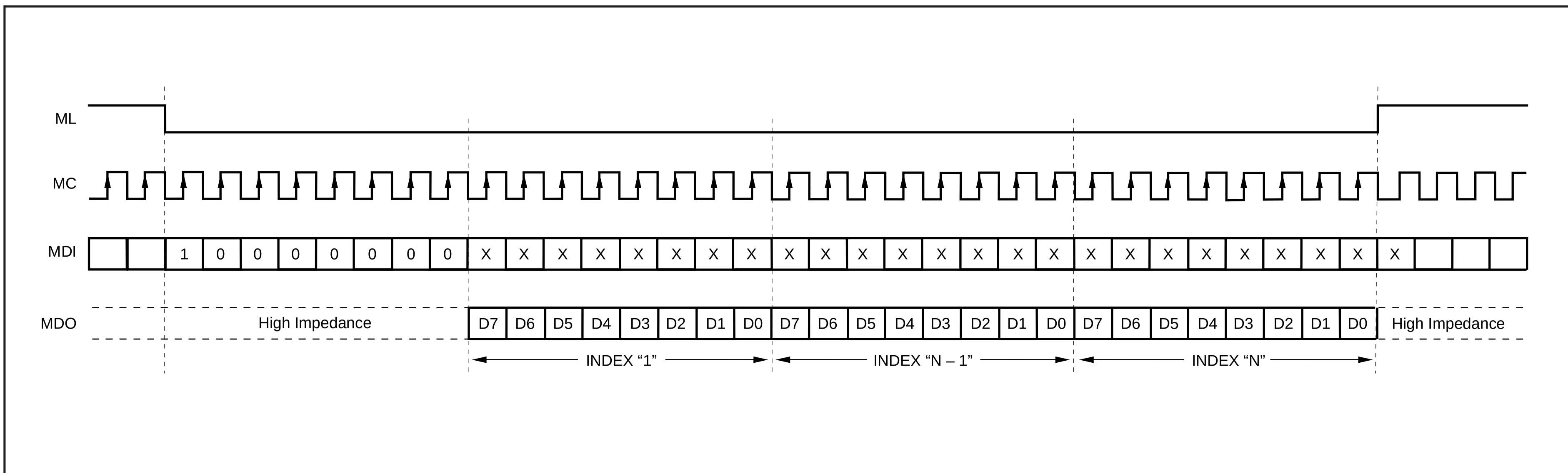


FIGURE 9. Read Operation Timing with INC = 1 (Auto-Increment Read).

last 8 bits of the 16-bit read cycle, which corresponds to the 8 data bits of the register indexed by the REG[6:0] bits of Control Register 11. The Read cycle is completed when ML is set to '1', immediately after the MC clock cycle for the least significant bit of indexed control register has completed.

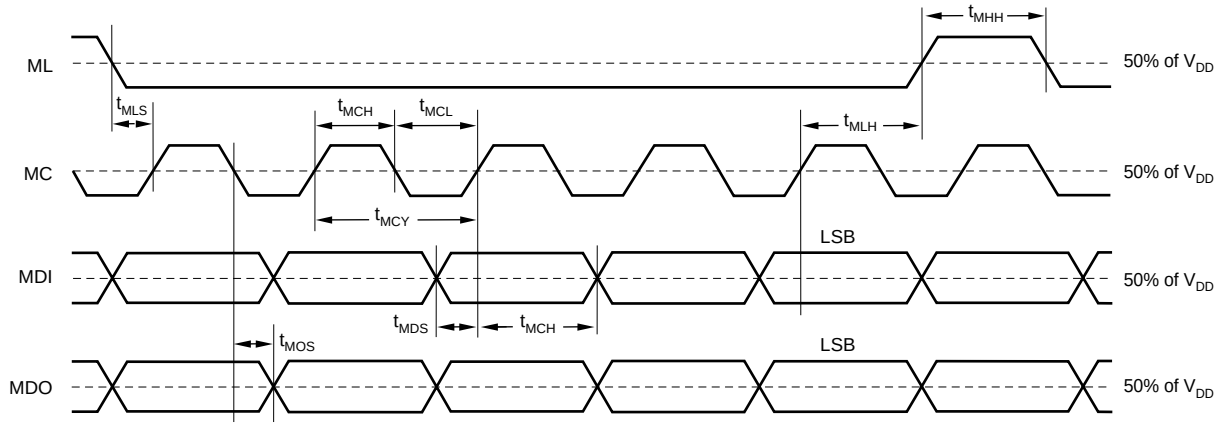
AUTO-INCREMENT READ OPERATION

The Auto-Increment Read function allows for multiple registers to be read sequentially. The Auto-Increment Read function is enabled by setting the INC bit of Control Register 11 to '1'. The sequence always starts with Register 1, and ends with the register indexed by the REG[6:0] bits in Control Register 11.

Figure 9 shows the timing for the Auto-Increment Read operation. The operation begins by writing Control Register 11, setting INC to '1' and setting REG[6:0] to the last register to be read in the sequence. The actual Read operation starts on the next HIGH to LOW transition of the ML pin. The Read cycle starts by setting the R/W bit of the control word to '1', and setting all of the IDX[6:0] bits to '0.'. All subsequent bits input on the MDI are ignored while ML is set to '0.' For the first 8 clocks of the Read cycle, MDO is set to a high-impedance state. This is followed by a sequence of 8-bit words, each corresponding to the data contained in Control Registers 1 through N, where N is defined by the REG[6:0] bits in Control Register 11. The Read cycle is completed when ML is set to '1', immediately after the MC clock cycle for the least significant bit of Control Register N has completed.

CONTROL INTERFACE TIMING REQUIREMENTS

Figure 10 shows a detailed timing diagram for the Serial Control interface. Pay special attention to the setup and hold times, as well as t_{MLS} and t_{MLH}, which define minimum delays between edges of the ML and MC clocks. These timing parameters are critical for proper control port operation.



SYMBOL	PARAMETER	MIN	MAX	UNITS
t_{MCY}	MC Pulse Cycle Time	100		ns
t_{MCL}	MC Low Level Time	50		ns
t_{MCH}	MC High Level Time	50		ns
t_{MHH}	ML High Level Time	300		ns
t_{MLS}	ML Falling Edge to MC Rising Edge	20		ns
t_{MLH}	ML Hold Time(1)	20		ns
t_{MDI}	Hold Time	15		ns
t_{MDS}	MDL Set Up Time	20		ns
t_{MOS}	MC Falling Edge to MDSO Stable		30	ns

NOTE: (1) MC rising edge for LSB to ML rising edge.

FIGURE 10. Control Interface Timing.

MODE CONTROL REGISTERS

User-Programmable Mode Controls

The PCM1604 includes a number of user-programmable functions which are accessed via control registers. The registers are programmed using the Serial Control Interface which was previously discussed in this data sheet. Table III lists the available mode control functions, along with their reset default conditions and associated register index.

Register Map

The mode control register map is shown in Table IV. Each register includes a R/W bit, which determines whether a register read (R/W =1) or write (R/W = 0) operation is performed. Each register also includes an index (or address) indicated by the IDX[6:0] bits.

FUNCTION	RESET DEFAULT	CONTROL REGISTER	INDEX, IDX[6:0]
Digital Attenuation Control, 0dB to –63dB in 0.5dB Steps	0dB, No Attenuation	1 through 6	01_H - 07_H
Digital Attenuation Load Control	Data Load Disabled	7	07_H
Digital Attenuation Rate Select	$2/f_S$	7	07_H
Soft Mute Control	Mute Disabled	7	07_H
DAC 1-6 Operation Control	DAC 1-6 Enabled	8	08_H
Infinite Zero Detect Mute	Disabled	8	08_H
Audio Data Format Control	24-Bit Standard Format	9	09_H
Digital Filter Roll-Off Control	Sharp Roll-Off	9	09_H
SCKO Frequency Selection	Full Rate (= f_{SCKI})	9	09_H
SCKO Output Enable	SCKO Enabled	9	09_H
De-Emphasis Function Control	De-Emphasis Disabled	10	$0A_H$
De-Emphasis Sample Rate Selection	44.1kHz	10	$0A_H$
Output Phase Reversal	Disabled	10	$0A_H$
Read Register Index Control	REG[6:0] = 01_H	11	$0B_H$
Read Auto-Increment Control	Auto-Increment Disabled	11	$0B_H$
General Purpose Output Enable	Zero Flags Enabled	12	$0C_H$
General Purpose Output Bits (GPO1-GPO6)	Disabled	12	$0C_H$
Oversampling Rate Control	64x (32x for 192kHz)	12	$0C_H$

TABLE III. User-Programmable Mode Controls.

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 0	R/W	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
Register 1	R/W	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT17	AT16	AT15	AT14	AT13	AT12	AT11	AT10
Register 2	R/W	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT27	AT26	AT25	AT24	AT23	AT22	AT21	AT20
Register 3	R/W	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT37	AT36	AT35	AT34	AT33	AT32	AT31	AT30
Register 4	R/W	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT47	AT46	AT45	AT44	AT43	AT42	AT41	AT40
Register 5	R/W	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT57	AT56	AT55	AT54	AT53	AT52	AT51	AT50
Register 6	R/W	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT67	AT66	AT65	AT64	AT63	AT62	AT61	AT60
Register 7	R/W	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	ATLD	ATTS	MUT6	MUT5	MUT4	MUT3	MUT2	MUT1
Register 8	R/W	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	res	INZD	DAC6	DAC5	DAC4	DAC3	DAC2	DAC1
Register 9	R/W	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	res	res	FLT0	CLKD	CLKE	FMT2	FMT1	FMT0
Register 10	R/W	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	res	res	REV	DMF1	DMF0	DM56	DM34	DM12
Register 11	R/W	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	INC	REG6	REG5	REG4	REG3	REG2	REG1	REG0
Register 12	R/W	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	OVER	GPOE	GPO6	GPO5	GPO4	GPO3	GPO2	GPO1

TABLE IV. Mode Control Register Map.

REGISTER DEFINITIONS

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 1	R/W	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT17	AT16	AT15	AT14	AT13	AT12	AT11	AT10
Register 2	R/W	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT27	AT26	AT25	AT24	AT23	AT22	AT21	AT20
Register 3	R/W	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT37	AT36	AT35	AT34	AT33	AT32	AT31	AT30
Register 4	R/W	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT47	AT46	AT45	AT44	AT43	AT42	AT41	AT40
Register 5	R/W	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT57	AT56	AT55	AT54	AT53	AT52	AT51	AT50
Register 6	R/W	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT67	AT66	AT65	AT64	AT63	AT62	AT61	AT60

R/W **Read/Write Mode Select**

When R/W = 0, a Write operation is performed.

When R/W = 1, a Read operation is performed.

Default Value: 0

ATx[7:0] **Digital Attenuation Level Setting**

where x = 1-6, corresponding to the DAC output $V_{OUT}x$.

These bits are Read/Write.

Default Value: $1111\ 1111_B$

Each DAC output, $V_{OUT}1$ through $V_{OUT}6$, has a digital attenuator associated with it. The attenuator may be set from 0dB to –63dB, in 0.5dB steps. Alternatively, the attenuator may be set to infinite attenuation (or mute).

The attenuation data for each channel can be set individually. However, the data load control (ATLD bit of Control Register 7) is common to all six attenuators. ATLD must be set to '1' in order to change an attenuator's setting. The attenuation level may be set using the formula below.

Attenuation Level (dB) = 0.5 $(ATx\ [7:0]_{DEC} - 255)$

where: $ATx\ [7:0]_{DEC}$ = 0 through 255

for: $ATx\ [7:0]_{DEC}$ = 0 through 128, the attenuator is set to infinite attenuation.

The following table shows attenuator levels for various settings.

ATx[7:0]	Decimal Value	Attenuator Level Setting
$1111\ 1111_B$	255	0dB, No Attenuation (default)
$1111\ 1110_B$	254	–0.5dB
$1111\ 1101_B$	253	–1.0dB
•	•	•
•	•	•
•	•	•
$1000\ 0010_B$	130	–62.5dB
$1000\ 0001_B$	129	–63.0dB
$1000\ 0000_B$	128	Mute
•	•	•
•	•	•
•	•	•
$0000\ 0000_B$	0	Mute

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 7	R/W	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	ATLD	ATTS	MUT6	MUT5	MUT4	MUT3	MUT2	MUT1

R/W **Read/Write Mode Select**

When R/W = 0, a Write operation is performed.

When R/W = 1, a Read operation is performed.

Default Value: 0

ATLD **Attenuation Load Control**

This bit is Read/Write.

Default Value: 0

ATLD = 0	Attenuation Control Disabled (default)
ATLD = 1	Attenuation Control Enabled

The ATLD bit is used to enable loading of attenuation data set by registers 1 through 6. When ATLD = 0, the attenuation settings remain at the previously programmed level, ignoring new data loaded to registers 1 through 6. When ATLD = 1, attenuation data written to registers 1 through 6 is loaded normally.

ATTS **Attenuation Rate Select**

This bit is Read/Write.

Default Value: 0

ATTS = 0	Attenuation rate is $2/f_S$ (default)
ATTS = 1	Attenuation rate is $4/f_S$

Changes in attenuator levels are made by incrementing or decrementing the attenuator by one step (0.5dB) for every $2/f_S$ or $4/f_S$ time interval until the programmed attenuator setting is reached. This helps to minimize audible 'clicking', or zipper noise, while the attenuator is changing levels. The ATTS bit allows you to select the rate at which the attenuator is decremented/incremented during level transitions.

MUTx **Soft Mute Control**

where x = 1-6, corresponding to the DAC output $V_{OUT}x$.

These bits are Read/Write.

Default Value: 0

MUTx = 0	Mute Disabled (default)
MUTx = 1	Mute Enabled

The mute bits, MUT1 through MUT6, are used to enable or disable the Soft Mute function for the corresponding DAC outputs, $V_{OUT}1$ through $V_{OUT}6$. The Soft Mute function is incorporated into the digital attenuators. When Mute is disabled (MUTx = 0), the attenuator and DAC operate normally. When Mute is enabled by setting MUTx = 1, the digital attenuator for the corresponding output will be decremented from the current setting to the infinite attenuation setting one attenuator step (0.5dB) at a time, with the rate of change programmed by the ATTS bit. This provides a quiet, 'pop' free muting of the DAC output. Upon returning from Soft Mute, by setting MUTx = 0, the attenuator will be incremented one step at a time to the previously programmed attenuator level.

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
REGISTER 8	R/W	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	res	INZD	DAC6	DAC5	DAC4	DAC3	DAC2	DAC1

R/W **Read/Write Mode Select**

When R/W = 0, a Write operation is performed.

When R/W = 1, a Read operation is performed.

Default Value: 0

INZD **Infinite Zero Detect Mute Control**

This bit is Read/Write.

Default Value: 0

INZD = 0	Infinite Zero Detect Mute Disabled (default)
INZD = 1	Infinite Zero Detect Mute Enabled

The INZD bit is used to enable or disable the Zero Detect Mute function described in the Zero Flag and Infinite Zero Detect Mute section in this data sheet. The Zero Detect Mute function is independent of the Zero Flag output operation, so enabling or disabling the INZD bit has no effect on the Zero Flag outputs (ZERO1-ZERO6, ZEROA).

DACx **DAC Operation Control**

where x = 1-6, corresponding to the DAC output $V_{OUT}x$.

These bits are Read/Write.

Default Value: 0

DACx = 0	DAC Operation Enabled (default)
DACx = 1	DAC Operation Disabled

The DAC operation controls are used to enable and disable the DAC outputs, $V_{OUT}1$ through $V_{OUT}6$. When DACx = 0, the output amplifier input is connected to the DAC output. When DACx = 1, the output amplifier input is switched to the DC common-mode voltage ($V_{COM}1$ or $V_{COM}2$), equal to $V_{CC}/2$.

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
REGISTER 9	R/W	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	res	res	FLT0	CLKD	CLKE	FMT2	FMT1	FMT0

R/W **Read/Write Mode Select**

When R/W = 0, a Write operation is performed.
When R/W = 1, a Read operation is performed.
Default Value: 0

FLT0 **Digital Filter Roll-Off Control**

These bits are Read/Write.
Default Value: 000_B

FLT0 = 0	Sharp Roll-Off (default)
FLT0 = 1	Slow Roll-Off

Bit FLT0 allows the user to select the digital filter roll-off that is best suited to their application. Two filter roll-off sections are available: Sharp or Slow. The filter responses for these selections are shown in the Typical Performance Curves section of this data sheet.

CLKD **SCKO Frequency Selection**

This bit is Read/Write.
Default Value: 0

CLKD = 0	Full Rate, $f_{SCKO} = f_{SCKI}$ (default)
CLKD = 1	Half Rate, $f_{SCKO} = f_{SCKI}/2$

The CLKD bit is used to determine the clock frequency at the system clock output pin, SCKO.

CLKE **SCKO Output Enable**

This bit is Read/Write.
Default Value: 0

CLKE = 0	SCKO Enabled (default)
CLKE = 1	SCKO Disabled

The CLKE bit is used to enable or disable the system clock output pin, SCKO. When SCKO is enabled, it will output either a full or half rate clock, based upon the setting of the CLKD bit.

FMT[2:0] **Audio Interface Data Format**

These bits are Read/Write.
Default Value: 000_B

FMT[2:0]	Audio Data Format Selection
000	24-Bit Standard Format, Right-Justified Data (default)
001	20-Bit Standard Format, Right-Justified Data
010	18-Bit Standard Format, Right-Justified Data
011	16-Bit Standard Format, Right-Justified Data
100	I^2S Format, 16- to 24-bits
101	Left-Justified Format, 16- to 24-Bits
110	Reserved
111	Reserved

The FMT[2:0] bits are used to select the data format for the serial audio interface.

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
REGISTER 10	R/W	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	res	res	REV	DMF1	DMF0	DM56	DM34	DM12

R/W **Read/Write Mode Select**

When R/W = 0, a Write operation is performed.
When R/W = 1, a Read operation is performed.
Default Value: 0

DMF[1:0] **Sampling Frequency Selection for the De-Emphasis Function**

These bits are Read/Write.
Default Value: 00_B

DMF[1:0]	De-Emphasis Same Rate Selection
00	44.1 kHz (default)
01	48 kHz
10	32 kHz
11	Reserved

The DMF[1:0] bits are used to select the sampling frequency used for the Digital De-Emphasis function when it is enabled. The de-emphasis curves are shown in the Typical Performance Curves section of this data sheet.

DM12 **Digital De-Emphasis Control for Channels 1 and 2**

This bit is Read/Write.
Default Value: 0

DM12 = 0	De-Emphasis Disabled for Channels 1 and 2 (default)
DM12 = 1	De-Emphasis Enabled for Channels 1 and 2

The DM12 bit is used to enable or disable the De-emphasis function for $V_{OUT}1$ and $V_{OUT}2$, which correspond to the Left and Right channels of the DATA1 input.

DM34 **Digital De-Emphasis Control for Channels 3 and 4**

This bit is Read/Write.
Default Value: 0

DM34 = 0	De-Emphasis Disabled for Channels 3 and 4 (default)
DM34 = 1	De-Emphasis Enabled for Channels 3 and 4

The DM34 bit is used to enable or disable the De-Emphasis function for $V_{OUT}3$ and $V_{OUT}4$, which correspond to the Left and Right channels of the DATA2 input.

DM56 **Digital De-Emphasis Control for Channels 5 and 6**

This bit is Read/Write.
Default Value: 0

DM56 = 0	De-Emphasis Disabled for Channels 5 and 6 (default)
DM56 = 1	De-Emphasis Enabled for Channels 5 and 6

The DM56 bit is used to enable or disable the de-emphasis function for $V_{OUT}5$ and $V_{OUT}6$, which correspond to the Left and Right channels of the DATA3 input.

REV **Output Phase Reversal**

This bit is Read/Write.
Default Value: 0

REV = 0	Normal Output (non-inverted)
REV = 1	Inverted Output

The REV bit is used to invert the output phase for $V_{OUT}1$ through $V_{OUT}6$. When the REV bit is enabled, the zero-detect functions (including zero-detect mute and the zero flags) are not available.

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
REGISTER 11	R/W	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	INC	REG6	REG5	REG4	REG3	REG2	REG1	REG0

R/W **Read/Write Mode Select**

When R/W = 0, a Write operation is performed.

When R/W = 1, a Read operation is performed.

Default Value: 0

INC **Auto-Increment Read Control**

This bit is Read/Write.

Default Value: 0

INC = 0	Auto-Increment Read Disabled (default)
INC = 1	Auto-Increment Read Enabled

The INC bit is used to enable or disable the Auto-Increment Read feature of the Serial Control Interface. Refer to the Serial Control Interface section of this data sheet for details regarding Auto-Increment Read operation.

REG[6:0] **Read Register Index**

These bits are Read/Write.

Default Value: 01_H

Bits REG[6:0] are used to set the index of the register to be read when performing a Single Register Read operation. In the case of an Auto-Increment Read operation, bits REG[6:0] indicate the index of the last register to be read in the in the Auto-Increment Read sequence. For example, if Registers 1 through 6 are to be read during an Auto-Increment Read operation, bits REG[6:0] would be set to 06_H.

Refer to the Serial Control Interface section of this data sheet for details regarding the Single Register and Auto-Increment Read operations.

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
REGISTER 12	R/W	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	OVER	GPOE	GPO6	GPO5	GPO4	GPO3	GPO2	GPO1

GPOx **General Purpose Logic Output**

Where: x = 1 through 6, corresponding to pins GPO1 through GPO6.

These bits are Read/Write.

Default Value: 0

GPOx = 0	Set GPOx to '0'.
GPOx = 1	Set GPOx to '1'.

The general-purpose output pins, GPO1 through GPO6, are enabled by setting GPOE = 1. These pins are used as general-purpose outputs for controlling user-defined logic functions. When general-purpose outputs are disabled (GPOE = 0), they default to the zero-flag function, ZERO1 through ZERO6.

GPOE **General Purpose Output Enable**

This bit is Read/Write.

Default Value: 0

GPOE = 0	General-Purpose Outputs Disabled. Pins default to zero-flag function (ZERO1 through ZERO6).
GPOE = 1	General-Purpose Outputs Enabled. Data written to GPO1 through GPO6 will appear at the corresponding pins.

OVER **Oversampling Rate Control**

This bit is Read/Write.

Default Value: 0

OVER = 0	64x oversampling for $f_S \leq 96kHz$, and 32x oversampling for $f_S > 96kHz$.
OVER = 1	128x oversampling for $f_S \leq 96kHz$, and 64x oversampling for $f_S > 96kHz$.

The OVER bit is utilized to control the total oversampling performed by the D/A converter, including the digital interpolation filter and delta-sigma DAC. This is useful for controlling the D/A out-of-band noise spectrum, and designing a single, fixed value low-pass filter for use with all sampling frequencies.

ANALOG OUTPUTS

The PCM1604 includes six independent output channels, $V_{OUT}1$ through $V_{OUT}6$. These are unbalanced outputs, each capable of driving 3.1Vp-p typical into a 5kΩ AC load with V_{CC} = +5V. The internal output amplifiers for $V_{OUT}1$ through $V_{OUT}6$ are DC biased to the common-mode (or bipolar zero) voltage, equal to $V_{CC}/2$.

The output amplifiers include a RC continuous-time filter, which helps to reduce the out-of-band noise energy present at the DAC outputs due to the noise shaping characteristics of the PCM1604's delta-sigma D/A converters. The frequency response of this filter is shown in Figure 11. By itself, this filter is not enough to attenuate the out-of-band noise to an acceptable level for most applications. An external low-pass filter is required to provide sufficient out-of-band noise rejection. Further discussion of DAC post-filter circuits is provided in the Applications Information section of this data sheet.

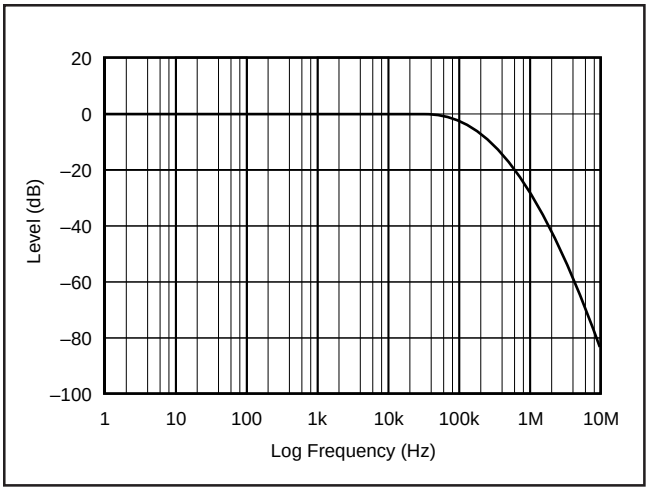


FIGURE 11. Output Filter Frequency Response.

$V_{COM}1$ AND $V_{COM}2$ OUTPUTS

Two unbuffered common-mode voltage output pins, $V_{COM}1$ (pin 16) and $V_{COM}2$ (pin 15), are brought out for decoupling purposes. These pins are nominally biased to a DC voltage level equal to $V_{CC}/2$. If these pins are to be used to bias external circuitry, a voltage follower is required for buffering purposes. Figure 12 shows an example of using the $V_{COM}1$ and $V_{COM}2$ pins for external biasing applications.

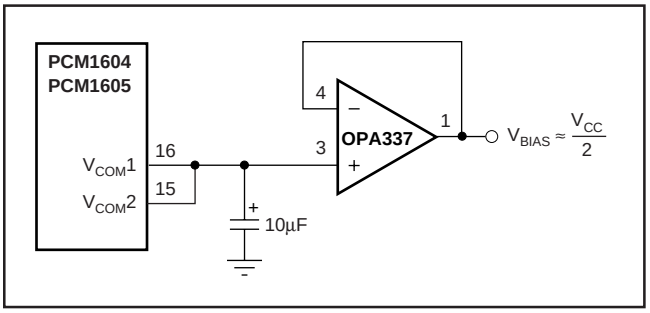


FIGURE 12. Biasing External Circuits Using the $V_{COM}1$ and $V_{COM}2$ Pins.

ZERO FLAG AND INFINITE ZERO DETECT MUTE FUNCTIONS

The PCM1604 includes circuitry for detecting an all '0' data condition for the data input pins, DATA1 through DATA3. This includes two independent functions: Zero Output Flags and Zero Detect Mute.

Although the flag and mute functions are independent of one another, the zero detection mechanism is common to both functions.

Zero Detect Condition

Zero Detection for each output channel is independent from the others. If the data for a given channel remains at a '0' level for 1024 sample periods (or LRCK clock periods), a Zero Detect condition exists for the that channel.

Zero Output Flags

Given that a Zero Detect condition exists for one or more channels, the Zero flag pins for those channels will be set to a logic '1'state. There are Zero Flag pins for each channel, ZERO1 through ZERO6 (pins 1 through 6). In addition, all six Zero Flags are logically ANDed together and the result provided at the ZEROA pin (pin 48), which is set to a logic '1' state when all channels indicate a zero detect condition. The Zero Flag pins can be used to operate external mute circuits, or used as status indicators for a microcontroller, audio signal processor, or other digitally controlled functions.

Infinite Zero Detect Mute

Infinite Zero Detect Mute is an internal logic function. The Zero Detect Mute can be enabled or disabled using the INZD bit of Control Register 8. The reset default is Zero Detect Mute disabled, INZD = 0. Given that a Zero Detect Condition exists for one or more channels, the zero mute circuitry will immediately force the corresponding DAC output(s) to the bipolar zero level, or $V_{CC}/2$. This is accomplished by switching the input of the DAC output amplifier from the delta-sigma modulator output to the DC common-mode reference voltage.

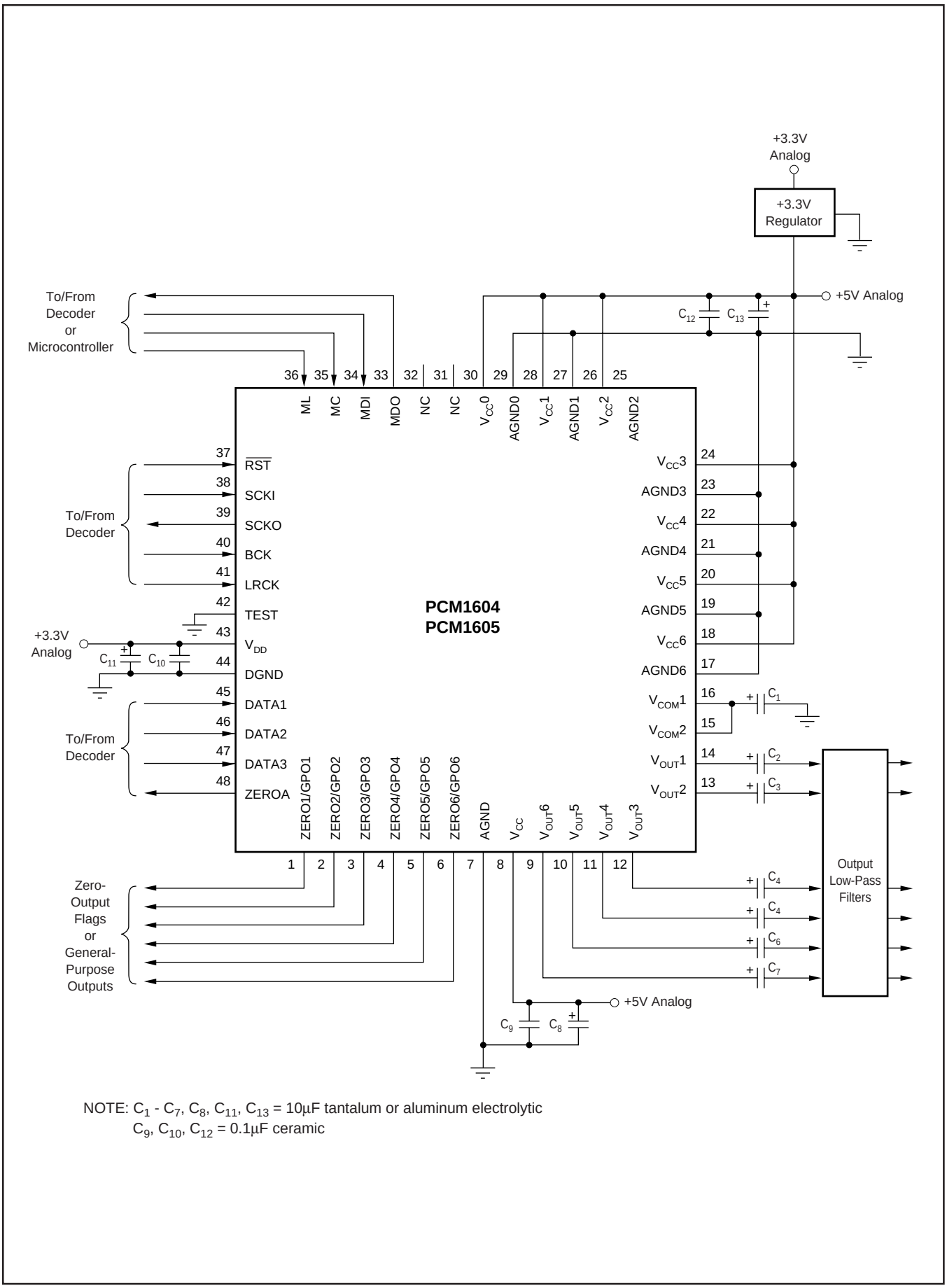
APPLICATIONS INFORMATION

CONNECTION DIAGRAMS

A basic connection diagram is shown in Figure 13, with the necessary power supply bypassing and decoupling components. Burr-Brown recommends using the component values shown in Figure 13 for all designs.

A typical application diagram is shown in Figure 14. Burr-Brown's REG1117-3.3 is used to generate +3.3V for V_{DD} from the +5V analog power supply. Burr-Brown's PLL1700E is used to generate the system clock input at SCKI, as well as generating the clock for the audio signal processor.

The use of series resistors (22Ω to 100Ω) are recommended for SCKI, LRCK, BCK, DATA1, DATA2, and DATA3. The series resistor combines with the stray PCB and device input capacitance to form a low-pass filter which removes high frequency noise from the digital signal, thus reducing high frequency emission.



NOTE: C_1 - C_7, C_8, C_{11}, C_{13} = 10µF tantalum or aluminum electrolytic
C_9, C_{10}, C_{12} = 0.1µF ceramic

FIGURE 13. Basic Connection Diagram.

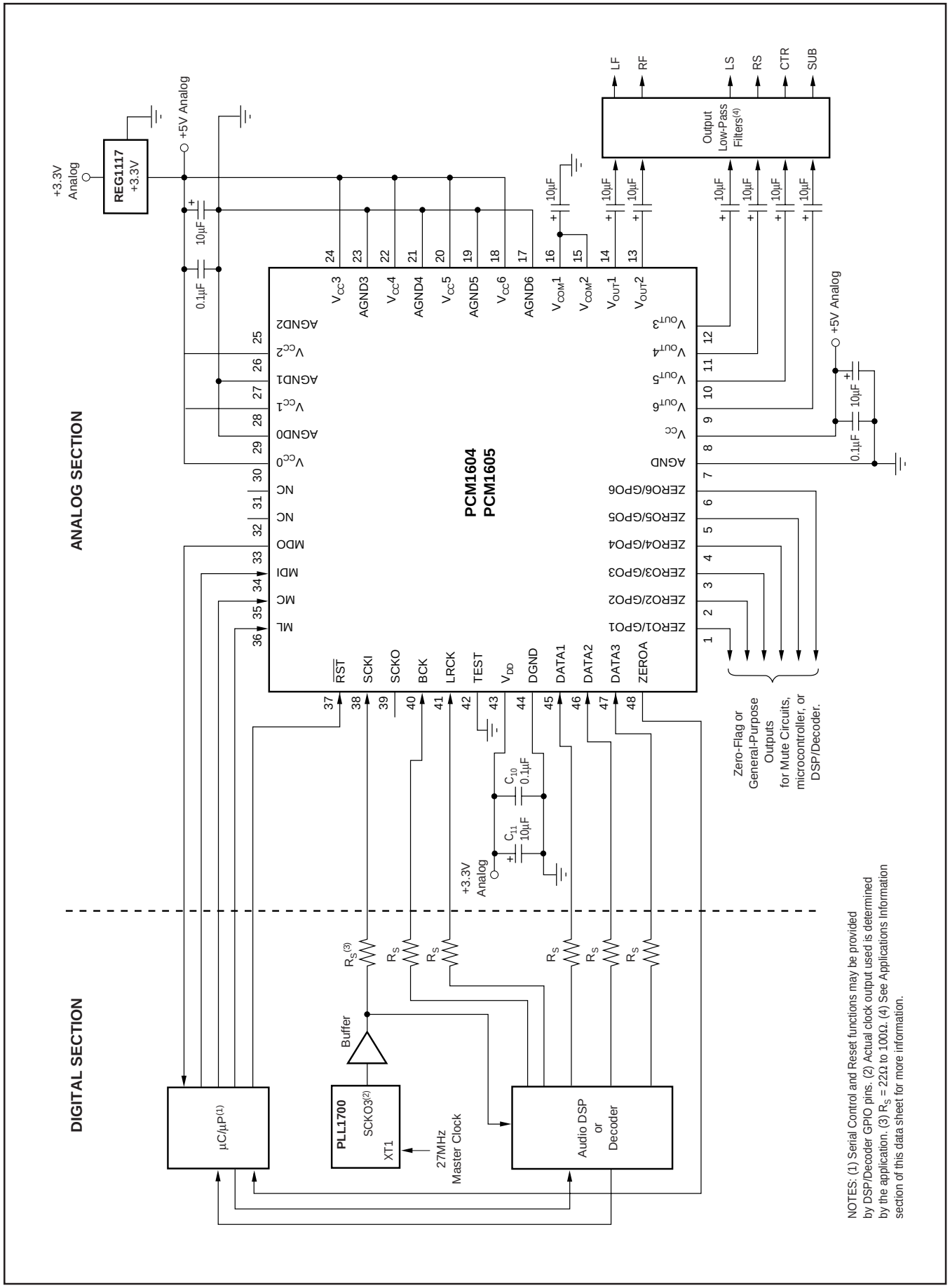


FIGURE 14. Typical Application Diagram.

POWER SUPPLIES AND GROUNDING

The PCM1604 requires a +5V analog supply and a +3.3V digital supply. The +5V supply is used to power the DAC analog and output filter circuitry, while the +3.3V supply is used to power the digital filter and serial interface circuitry. For best performance, the +3.3V supply should be derived from the +5V supply using a linear regulator, as shown in Figure 14.

Six capacitors are required for supply bypassing, as shown in Figure 13. These capacitors should be located as close as possible to the PCM1604 or PCM1605 package. The 10µF capacitors should be tantalum or aluminum electrolytic, while the 0.1µF capacitors are ceramic (X7R type is recommended for surface-mount applications).

D/A OUTPUT FILTER CIRCUITS

Delta-sigma D/A converters utilize noise shaping techniques to improve in-band Signal-to-Noise Ratio (SNR) performance at the expense of generating increased out-of-band noise above the Nyquist Frequency, or $f_S/2$. The out-of-band noise must be low-pass filtered in order to provide the optimal converter performance. This is accomplished by a combination of on-chip and external low-pass filtering.

Figures 15 and 16 show the recommended external low-pass active filter circuits for dual and single-supply applications. These circuits are 2nd-order Butterworth filters using the Multiple Feedback (MFB) circuit arrangement, which reduces sensitivity to passive component variations over frequency and temperature. For more information regarding MFB active filter design, please refer to Burr-Brown Applications Bulletin AB-034, available from our web site (www.burr-brown.com) or your local Burr-Brown sales office.

Since the overall system performance is defined by the quality of the D/A converters and their associated analog output circuitry, high quality audio op amps are recommended for the active filters. Burr-Brown's OPA2134 and OPA2353 dual op amps are shown in Figures 15 and 16, and are recommended for use with the PCM1604 and PCM1605.

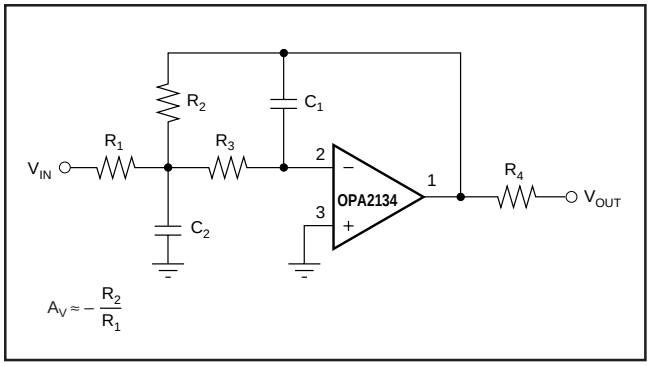


FIGURE 15. Dual Supply Filter Circuit.

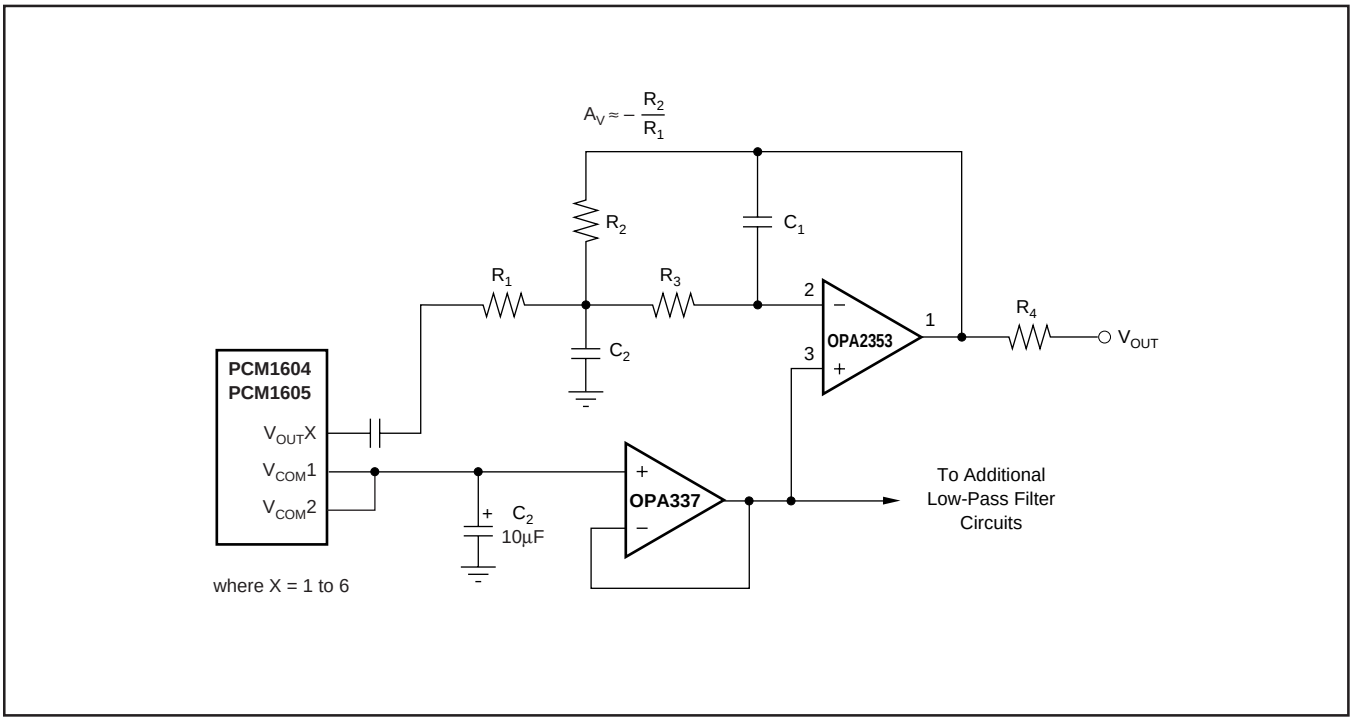


FIGURE 16. Single-Supply Filter Circuit.

PCB LAYOUT GUIDELINES

A typical PCB floor plan for the PCM1604 and PCM1605 is shown in Figure 17. A ground plane is recommended, with the analog and digital sections being isolated from one another using a split or cut in the circuit board. The PCM1604 or PCM1605 should be oriented with the digital I/O pins facing the ground plane split/cut to allow for short, direct connections to the digital audio interface and control signals originating from the digital section of the board.

Separate power supplies are recommended for the digital and analog sections of the board. This prevents the switching noise present on the digital supply from contaminating the analog power supply and degrading the dynamic performance of the D/A converters. In cases where a common +5V supply must be used for the analog and digital sections, an inductance (RF choke, ferrite bead) should be placed between the analog and digital +5V supply connections to avoid coupling of the digital switching noise into the analog circuitry. Figure 18 shows the recommended approach for single-supply applications.

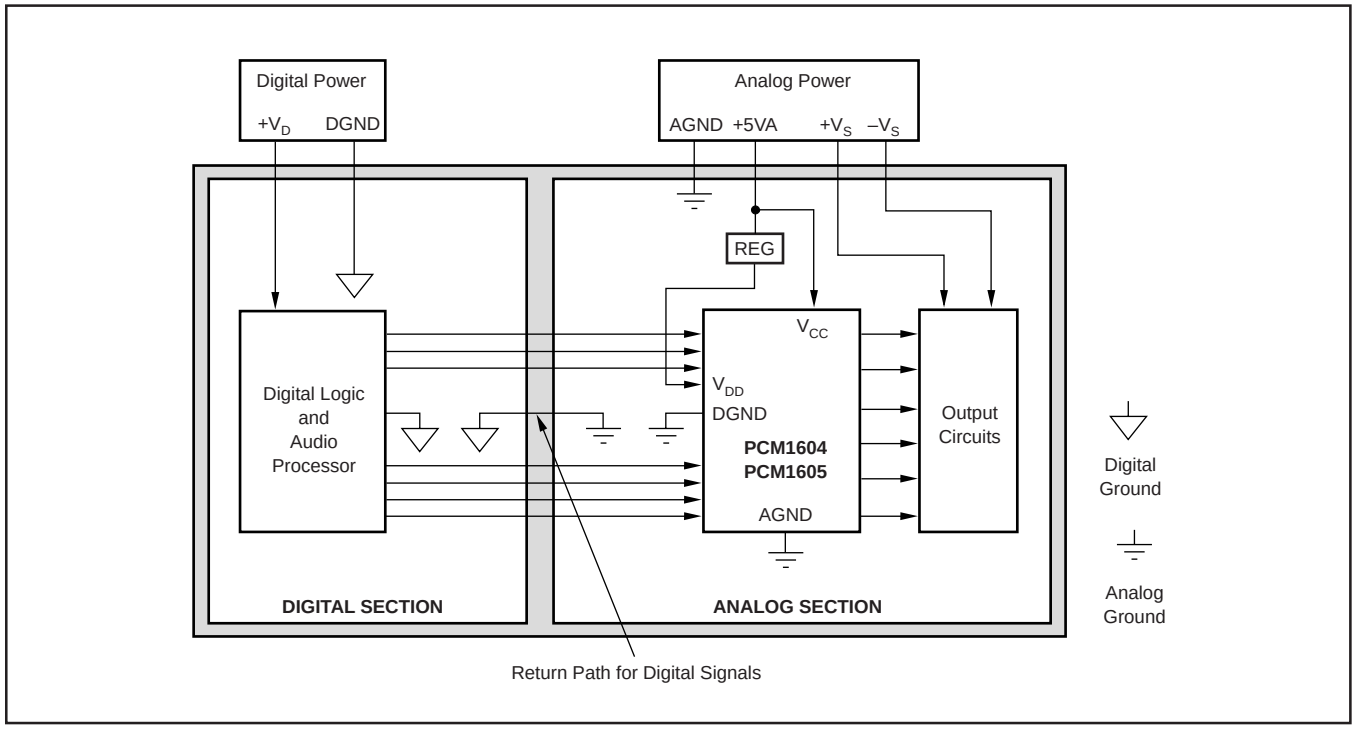


FIGURE 17. Recommended PCB Layout.

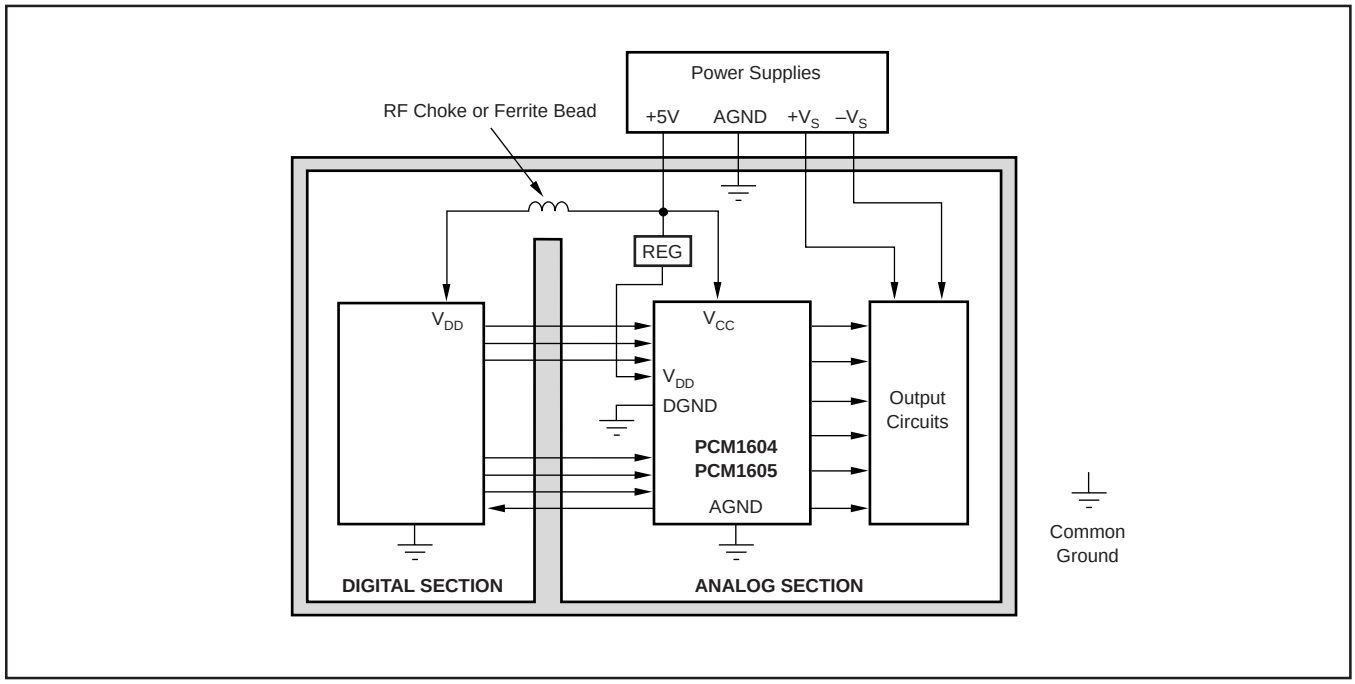


FIGURE 18. Single-Supply PCB Layout.

THEORY OF OPERATION

The D/A converter section of the PCM1604 is based upon a multi-bit delta-sigma architecture. This architecture utilizes an 4th-order noise shaper and an 8-level quantizer, followed by an analog low-pass filter. A block diagram of the delta-sigma modulator is shown in Figure 19. This architecture has the advantage of stability and improved jitter tolerance when compared to traditional 1-bit (2-level) delta-sigma designs.

The combined oversampling rate of the digital interpolation filter and the delta-sigma modulator is 32fs, 64fs, or 128fs. The total oversampling rate is determined by the desired sampling frequency. If fs ≤ 96kHz, then the OVER bit in Register 12 may be set to an oversampling rate to 64fs or 128fs. If fs > 96kHz, then the OVER bit may be used to set the oversampling rate to 32fs or 64fs. Figure 20 shows the out-of- band quantization noise plots for both the 64x and 128x oversampling scenarios. Notice that the 128x oversampling plot shows significantly improved out-of-band noise performance, allowing for a simplified low-pass filter to be used at the output of the DAC.

Figure 21 illustrates the simulated jitter sensitivity of the PCM1604. To achieve best performance, the system clock jitter should be less than 300 picoseconds. This is easily achieved using a quality clock generation IC, like Burr-Brown's PLL1700.

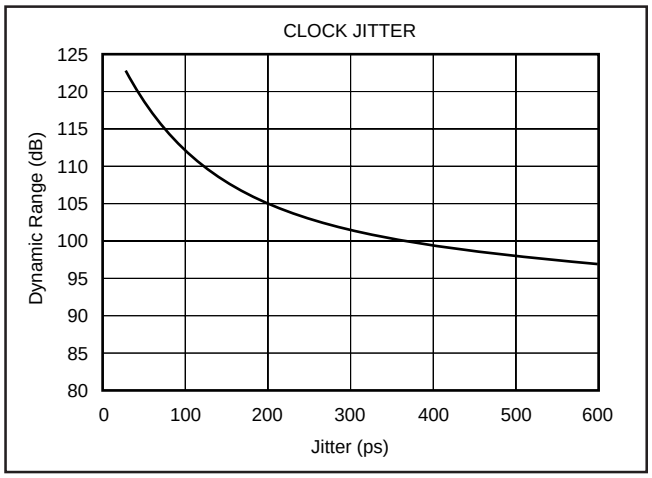


FIGURE 21. Jitter Sensitivity.

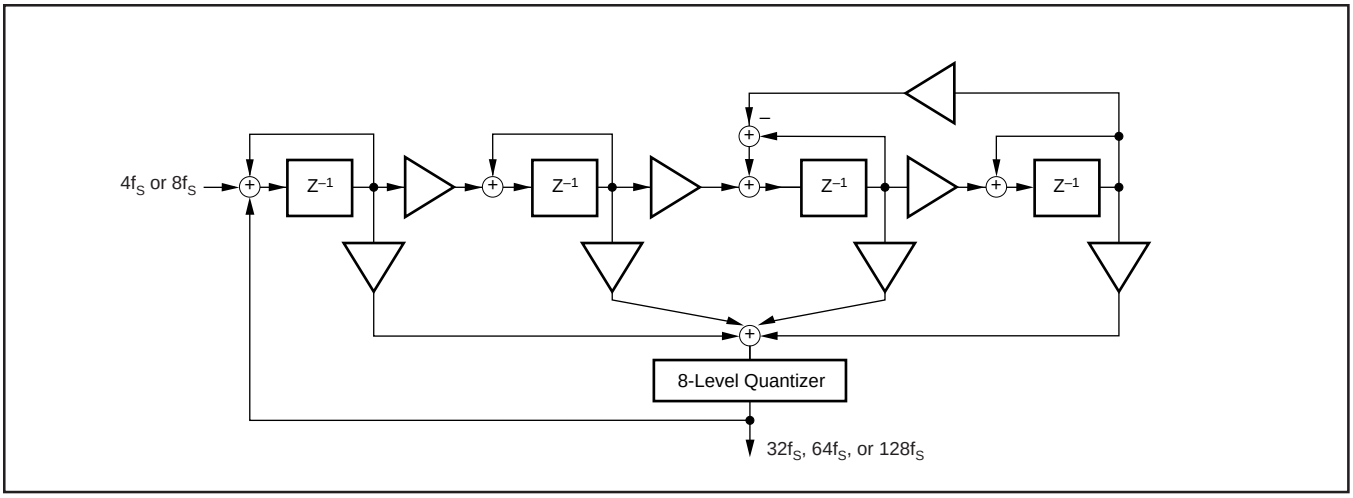


FIGURE 19. Eight-Level Delta-Sigma Modulator.

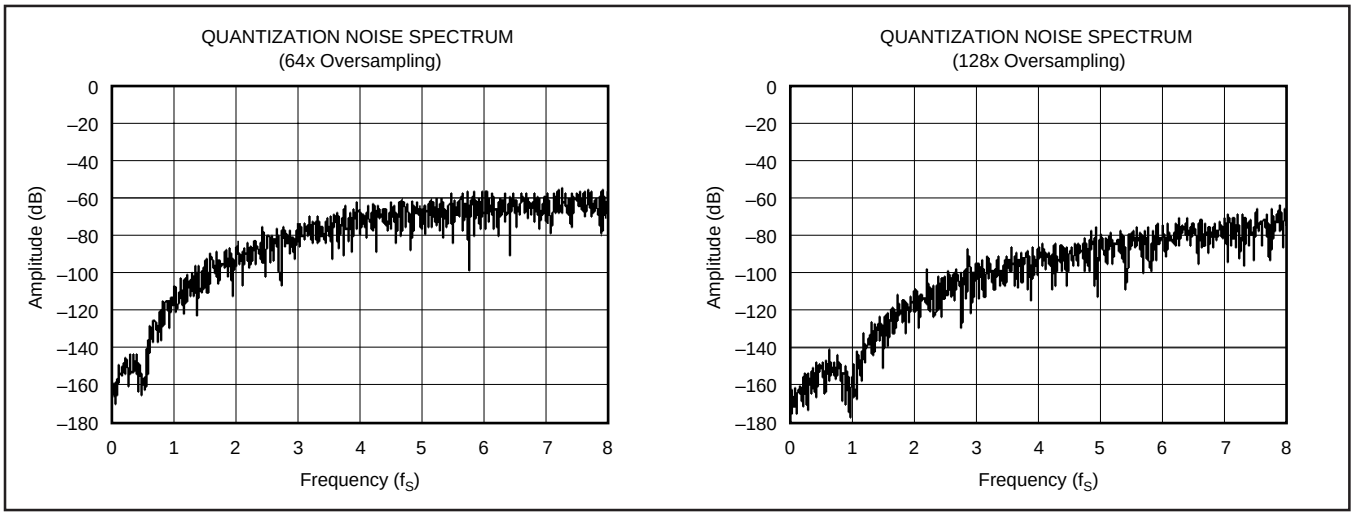


FIGURE 20. Quantization Noise Spectrum.

Not Recommended For New Designs

PERFORMANCE MEASUREMENTS

This section provides information on how to measure key dynamic performance parameters for the PCM1604 and PCM1605. In all cases, an Audio Precision System Two Cascade or equivalent audio measurement system is utilized to perform the testing.

TOTAL HARMONIC DISTORTION + NOISE

Total Harmonic Distortion + Noise (THD+N) is a significant figure of merit for audio D/A converters, since it takes into account both harmonic distortion and all noise sources within a specified measurement bandwidth. The true rms value of the distortion and noise is referred to as THD+N.

For the PCM1604 and PCM1605 D/A converters, THD+N is measured with a full scale, 1kHz digital sine wave as the test stimulus at the input of the DAC. The digital generator is set to 24-bit audio word length and a sampling frequency of 44.1kHz, or 96kHz. The digital generator output is taken from the unbalanced S/PDIF connector of the measurement system. The S/PDIF data is transmitted via coaxial cable to the digital audio receiver on the DEM-DAI1604 demo board. The receiver is then configured to output 24-bit data in either I^2S or left-justified data format. The DAC audio interface format is programmed to match the receiver output format. The analog output is then taken from the DAC post filter and connected to the analog analyzer input of the measurment system. The analog input is band limited using filters resident in the analyzer. The resulting THD+N is measured by the analyzer and displayed by the measurement system.

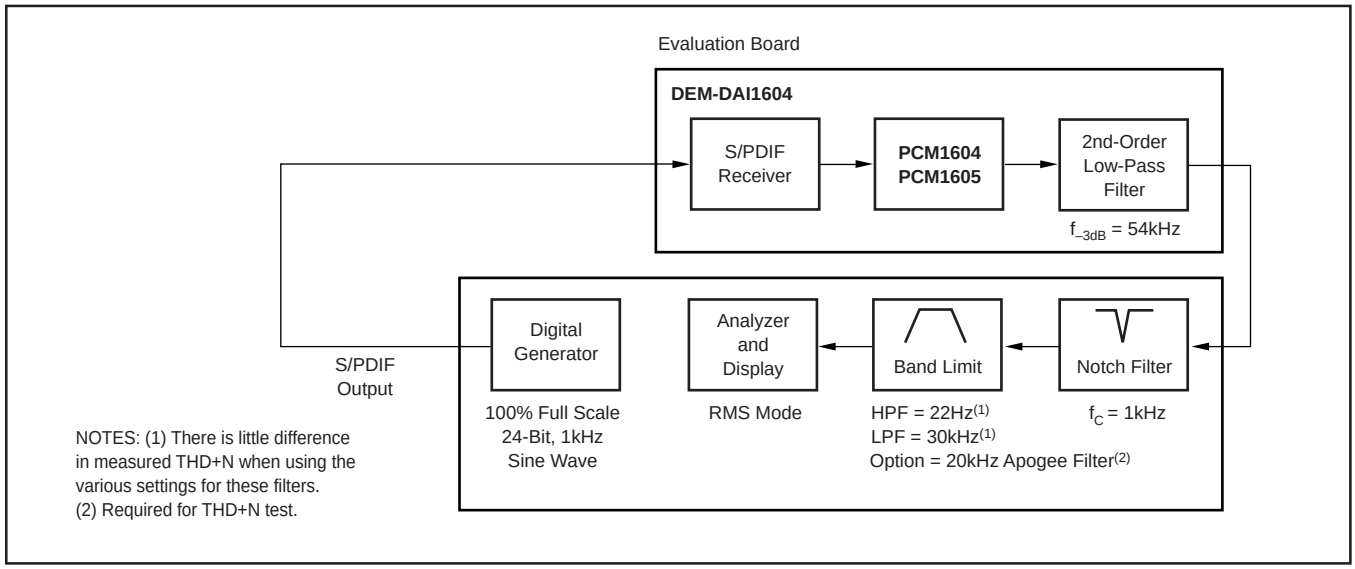


FIGURE 22. Test Setup for THD+N Measurements.

DYNAMIC RANGE

Dynamic range is specified as A-Weighted, THD+N measured with a –60dBFS, 1kHz digital sine wave stimulus at the input of the D/A converter. This measurment is designed to give a good indicator of how the DAC will perform given a low-level input signal.

The measurement setup for the dynamic range measurement is shown in Figure 23, and is similar to the THD+N test setup discussed previously. The differences include the band limit filter selection, the additional A-Weighting filter, and the –60dBFS input level.

IDLE CHANNEL SIGNAL-TO-NOISE RATIO

The SNR test provides a measure of the noise floor of the D/A converter. The input to the D/A is all 0's data, and the D/A converter's Infinite Zero Detect Mute function must be disabled (default condition at power up for the PCM1604, PCM1605). This ensures that the delta-sigma modulator output is connected to the output amplifier circuit so that idle tones (if present) can be observed and effect the SNR measurement. The dither function of the digital generator must also be disabled to ensure an all '0's data stream at the input of the D/A converter.

The measurement setup for SNR is identical to that used for dynamic range, with the exception of the input signal level (see the notes provided in Figure 23).

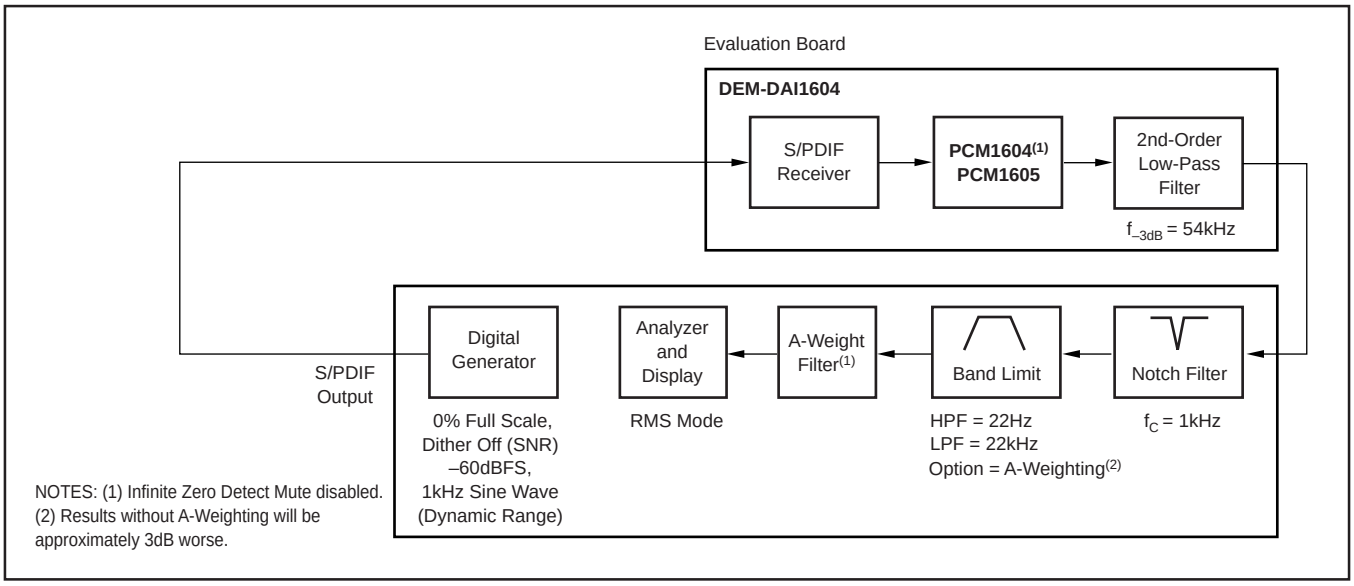


FIGURE 23. Test Set-Up for Dynamic Range and SNR Meeasurements.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PCM1604PTR	NRND	LQFP	PT	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		PCM1604	
PCM1604Y	NRND	LQFP	PT	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		PCM1604Y	
PCM1605Y	OBSOLETE	QFP	PJS	48		TBD	Call TI	Call TI			
PCM1605Y/1K	OBSOLETE	QFP	PJS	48		TBD	Call TI	Call TI			

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

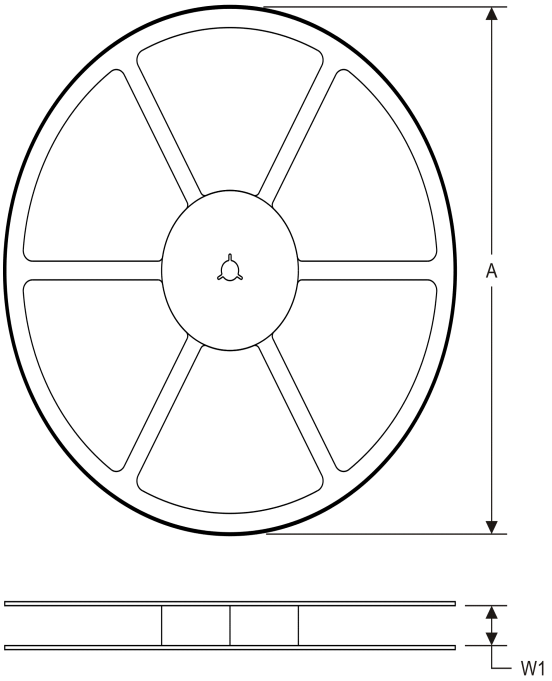
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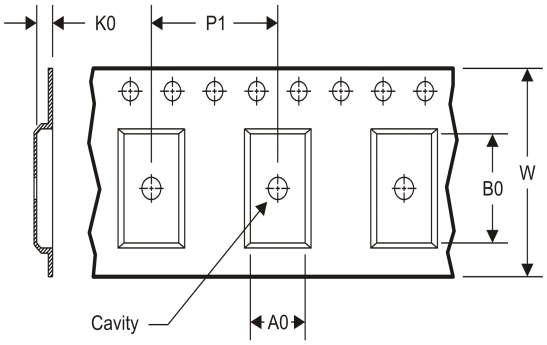
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TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



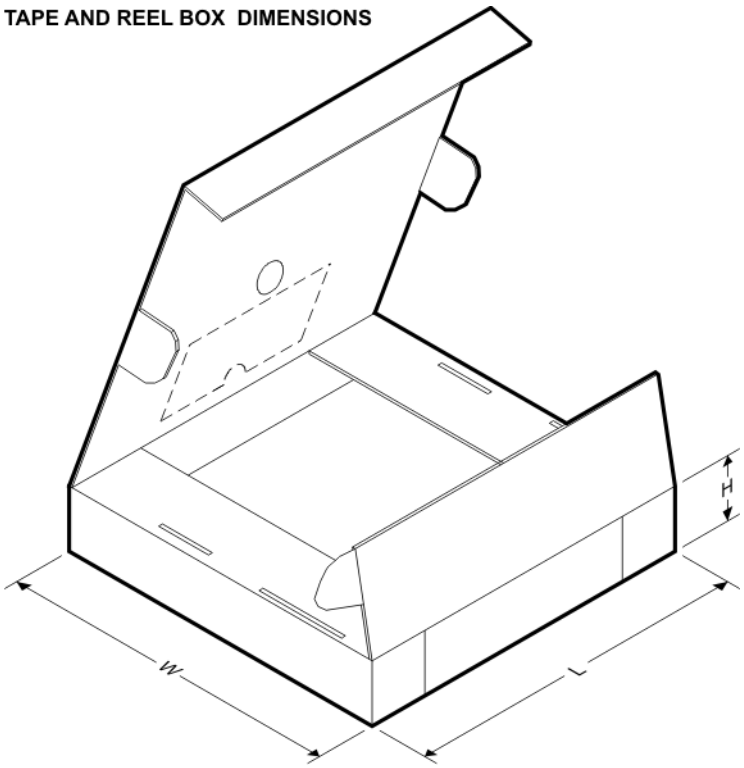
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCM1604PTR	LQFP	PT	48	1000	330.0	16.4	9.6	9.6	1.9	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCM1604PTR	LQFP	PT	48	1000	367.0	367.0	38.0

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